The Dissertation Committee for Yeonam Yoon
certifies that this is the approved version of the following dissertation:

# Low-power ADC designs in scaled CMOS process

Committee:

Nan Sun, Supervisor

T. R. Viswanathan

David Z. Pan

Michael Orshansky

Eric Soenen

# Low-power ADC designs in scaled CMOS process

**by**

**Yeonam Yoon, B.S.; M.S.**

**DISSERTATION**

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

**DOCTOR OF PHILOSOPHY**

THE UNIVERSITY OF TEXAS AT AUSTIN

May 2017

Dedicated to my parents and my wife.

# Acknowledgments

Most importantly, I would like to express my very special gratitude to my supervisor, Prof. Nan Sun. Without his continuous support and insightful guidance, I would have never accomplished my research works. He has inspired me with enthusiasm for research. Also, his generosity kept me moving forward. I would also like to thank my committee members, Prof. T. R. Viswanathan, Prof. David Z. Pan, Prof. Michael Orshansky, and Dr. Eric Soenen, for their valuable advice and discussions. I am truly grateful to Dr. Eric Soenen for giving a valuable opportunity for chip fabrication. I have been honored and thankful to my fellow students in Sun research group: Kareem Ragab, Arindam Sanyal, Long Chen, Wenjuan Guo, Sungjin Hong, Jeonggoo Song, Xiyuan Tang, Shaolan Li, Miguel Gandara, Linxiao Shen, and Abhishek Mukherjee. Special thanks to Arindam Sanyal, Sungjin Hong, Jeonggoo Song, Long Chen, and Wenjuan Guo for their collaboration in my research. I am greatly indebted to my parents for their selfless support and care. Last but by no means least, I am heartily thankful for having my wife, Sojeong Han in my life. I owe my deepest gratitude to her whose warm encouragement enabled me to go on with my research.

# Low-power ADC designs in scaled CMOS process

Yeonam Yoon, Ph.D.
The University of Texas at Austin, 2017

Supervisor: Nan Sun

This thesis presents advanced design techniques for successive approximation register (SAR) analog-to-digital converters (ADCs), continuous-time $\Delta\Sigma$ ADCs, and single-slope (SS) ADCs in nano-scale CMOS technologies.

(1) In high-speed SAR ADCs, metastability of the comparator limits the performance, which even results in the sparkle code errors. Proposed background calibration utilizing the comparator decision time detector removes the metastability-induced sparkle code errors by controlling the metastability detection window. At the same time, 1-bit resolution increase is gained from the proposed technique, which results in the fewer comparison cycles. Along with the relaxed requirement on the comparator, this cycle reduction helps to achieve the good power efficiency in high-speed SAR design. A prototype ADC in 40nm CMOS achieves 35.3dB SNDR and consumes 0.81mW while sampling at 700MS/s.

(2) In the proposed continuous-time $\Delta\Sigma$ ADCs, conventional power-hungry opamp is replaced by voltage controlled oscillators (VCOs) that perform the data

conversion in the phase domain instead of the voltage domain. In contrary to the opamp which is difficult to achieve good performance in the advanced CMOS process, VCOs have many advantages in the phase domain. To solve the nonlinear gain of VCOs, dual VCO-based integrator is used to suppress the dominant second-order distortion. To address the distortion from the DAC, a novel DAC calibration technique that both digitally senses and removes DAC mismatch errors is proposed. It has low hardware complexity by taking advantage of the intrinsic clocked level averaging (CLA) capability of dual-VCO-based integrator. It ensures high linearity regardless of the VCO center frequency. By lowering the VCO center frequency, power consumption is reduced. A prototype ADC designed in 130nm occupies an area of only $0.04mm^2$. It achieves 71dB SNDR over 1.7MHz bandwidth (BW) while sampling at 250MS/s and consuming only 0.9mW from a 1.2V power supply. The corresponding figure-of-merit (FOM) is 98 fJ/conversion-step.

(3) A SS ADC has advantages of high linearity and a simple architecture. Thus, it is well suited for the column-parallel architecture for the CMOS image sensors. However, conversion speed is severely limited in high-bit resolution since more than $2^N$ cycles are required for a N-bit resolution. To tackle this limitation, a two-step approach becomes popular. In this thesis, a two-step SAR/SS architecture is presented. In addition to reducing the conversion time, analog correlated double sampling (CDS) can cancel $kT/C$ noise, which enables capacitor area reduction. A prototype ADC in 180nm CMOS occupies only 9.3$\mu$m x 830$\mu$m. It achieves 60.5dB SNR after CDS while sampling at 256kHz and consuming 91$\mu$W.

# Table of Contents

# List of Tables

# List of Figures

# Chapter 1

# Introduction

## 1.1 Motivation

The demand for higher power efficiency has been increasing in many applications such as sensors or wireless communication as portable devices or Internet of Things (IoT) have been attracting lots of attention over the years. As an important interface between the analog world and the digital implementation, analog-to-digital converters (ADCs) also have been driven towards higher power efficiency. To this end, many techniques have been developed by researchers for various ADC architectures. Currently, pipeline, successive approximation register (SAR) and $\Delta\Sigma$ ADCs are dominant ADC architectures. In the specific application such as CMOS image sensors, single-slope (SS) ADCs are widely used.

In this thesis, advanced design techniques for a SAR ADC, a continuous-time $\Delta\Sigma$ ADC, and a SS ADC are presented. They are implemented differently in each ADC by (1) resolution enhancement while removing the sparkle code errors in the SAR ADC, (2) replacement of the conventional power-hungry component with voltage controlled oscillators (VCOs) along with the DAC calibration in the continuous-time $\Delta\Sigma$ ADC, and (3) conversion speed increase and $kT/C$ noise cancellation from two-step conversion by adopting SAR into the SS ADC.

SAR ADC is a popular choice due to its simple architecture and no need of opamps. In addition, due to the digital-friendly design nature, its bandwidth is increased as the technology scales, which broadens the application of SAR to high-speed data communication systems for higher power efficiency. Another requirement placed is the bit error rate (BER). Low BER is important for applications such as instrumentation. Therefore, a technique for high-speed SAR ADCs having low BER along with low power consumption is needed. This thesis presents a 6-b high-speed SAR ADC with sparkle code correction. By quantizing the comparator decision time (CDT), the sparkle codes are identified and corrected, reducing the error rate from $10^{-4}$ to below $10^{-9}$. Furthermore, CDT quantization enables 1-bit increase in the ADC resolution by setting the detection boundary to be $\pm$0.25 LSB. Thus, only 5 comparison cycles are needed to reach 6-b, leading to increased ADC speed. The DAC also only needs to be 5-b, resulting in reduced chip area and faster settling. A novel dither-based background calibration technique is devised to accurately control the CDT detection window size and ensure PVT robustness. A prototype ADC in 40nm CMOS achieves 35.3dB SNDR and consumes 0.81mW while sampling at 700MS/s.

Continuous-time $\Delta\Sigma$ ADCs gain popularity in the wide bandwidth application due to the following advantages. By taking advantage of the noise shaping from the oversampling, inaccurate components can be used along with the inherent anti-aliasing property, which makes the power-efficient design possible. However, in the advanced nanometer-scale CMOS process, conventional $\Delta\Sigma$ ADCs employing the operational transconductance amplifiers (OTA) encounter difficulties due to

the smaller gain and reduced signal swing. An emerging and promising approach to design $\Delta\Sigma$ ADCs is to use VCOs built with a ring of inverters. Ring VCOs act as both integrators and quantizers in the phase domain. Thus, they can replace OTA-based integrators and flash quantizers in conventional $\Delta\Sigma$ ADCs. Despite the many merits, VCO-based ADCs have one major limitation, which is VCO's nonlinear frequency tuning characteristic. Thus, it is desirable to develop power-efficient way to suppress the VCO's nonlinearity while taking advantage of the merits. In this thesis, a low-power and small-area VCO-based closed-loop $\Delta\Sigma$ ADC with two highlights is presented. First, the ADC has a distributed modular architecture. It consists of repetitive slices, which simplifies both schematic and layout design. It allows the ADC to be easily reconfigured for other resolution specifications. Second, a novel digital DAC mismatch calibration technique is proposed. It has low hardware complexity by taking advantage of the intrinsic clocked averaging (CLA) capability of dual VCO-based integrator. It ensures high linearity in the presence of large DAC mismatches. A prototype ADC in 130nm CMOS occupies only $0.04mm^2$ . It achieves 71dB SNDR over 1.7MHz BW while sampling at 250MS/s and consuming 0.9mW under a 1.2V supply. In addition, purely-VCO-based single-loop second-order continuous-time $\Delta\Sigma$ ADC is presented with the behavioral simulation. This exploits the pulse width modulation (PWM) property of the VCO-based integrator to build up the second-order modulator.

A SS ADC is widely used in column-parallel architectures in a CMOS image sensor (CIS). It offers good linearity and has a very simple architecture. It mainly consists of a single comparator with small area. However, conversion time

is a limiting factor in high-bit resolution since more than $2^N$ cycles are required for a N-bit resolution. 1-bit increase in the resolution makes the quantization period double. Therefore, for high resolution, it requires a fast clock speed, leading to the higher power consumption. To overcome this speed disadvantage, other ADC schemes for column-parallel architectures must be suggested. A column-parallel SAR/SS ADC exploiting $kT/C$ noise cancellation using analog correlated double sampling (CDS) for a CIS is presented. Inputs are quantized by SAR and SS sequentially in a two-step way. To reduce the capacitor area of SAR, which is the one of the main disadvantage, SS is added with minimal hardware change. Analog CDS is embraced to cancel the comparator offset. This is further extended to cancel the $kT/C$ noise in CDS mode. A prototype ADC in 180nm CMOS occupies only 9.3$\mu$m $\times$ 830$\mu$m. It achieves 60.5dB SNR after CDS while sampling at 256kHz and consuming 91$\mu$W.

## 1.2 Organization

Chapter 2 of the thesis presents a high-speed SAR ADC with the sparkle code reduction and resolution enhancement by the proposed dither-based background calibration using the comparator decision time quantizer. It also includes the measurement results of a prototype ADC designed in 40nm CMOS technology. Chapter 3 presents a continuous-time $\Delta\Sigma$ ADC with the VCO-based integrators to replace the power-hungry opamp. Distributed modular architecture is proposed with a novel DAC calibration. The measurement results for the prototype ADC designed in 180nm CMOS technology are also discussed. Behavioral simulation for

the second-order purely-VCO-based modulator is performed. Chapter 4 presents a two-step SAR/SS ADC for CIS to shorten the conversion time in the high-bit resolution. The measured results are also shown in Chapter 4. The conclusion is drawn in Chapter 5.

# Chapter 2

# Sparkle Code Correction and Resolution Enhancement in SAR

This chapter[1] presents a 6-b high-speed SAR ADC with sparkle code correction. By quantizing the comparator decision time (CDT), the sparkle codes are identified and corrected, reducing the error rate from $10^{-4}$ to below $10^{-9}$. Furthermore, CDT quantization enables 1-bit increase in the ADC resolution by setting the detection boundary to be $\pm 0.25$ LSB. Thus, only 5 comparison cycles are needed to reach 6-b, leading to increased ADC speed. The DAC also only needs to be 5-b, resulting in reduced chip area and faster settling. A novel dither-based background calibration technique is devised to accurately control the CDT detection window size and ensure PVT robustness. A prototype ADC in 40nm CMOS achieves 35.3dB SNDR and consumes 0.81mW while sampling at 700MS/s.

This chapter is organized as follows: an introduction is first presented. Design of the asynchronous SAR is explained and the sparkle code errors are analyzed next. The ADC design and the proposed technique are followed. Finally, the measurement results are shown, followed by the conclusion.

[1]This chapter is an extended work of the publication: Yeonam Yoon and Nan Sun, "A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration", *IEEE CICC*, accepted, 2017. I thank Dr. Nan Sun for his valuable advice in designing and testing of the prototypes.

## 2.1 Introduction

The demand for the higher power efficiency in high-speed low-to-moderate resolution applications such as wireless communication makes successive approximation register (SAR) analog-to-digital converters (ADCs) a popular choice. Due to the digital-friendly design nature, its bandwidth is increased as the technology scales, which broadens the application of SAR to high-speed data communication systems for higher power efficiency [Kull et al. [2014]]. Around 20 fJ per conversion step with higher-than 1GS/s sampling speed has been achieved with an effective number of bit (ENOB) below 11b [Chan et al. [2017a]; Lin et al. [2016]]. Another requirement placed is bit error rate (BER). Low BER is important for applications such as instrumentation. For example, WLAN and instrumentation requires BER to be lower than $10^{-9}$ and $10^{-12}$, respectively [Guhados et al. [2012]]. Bit errors occur from the sparkle codes due to the metastability of the comparator. Although the metastability does not degrade the ADC performance much in terms of SNDR since its occurrence is rare, complicated error correction is needed to meet the BER specification [Agazzi [2008]]. High-speed SAR ADC experiences the metastability issue more since less time is allocated to the comparator decision. Due to the importance, metastability in pipelined ADCs or various types of SAR ADCs was studied by researchers theoretically [Hashemi and Razavi [2014]; Waters et al. [2012]; Chan et al. [2017b]].

For a synchronous SAR ADC, metastability means the comparator cannot fully resolve within one comparison cycle, causing wrong outputs. For an asynchronous SAR ADC [Chen and Brodersen [2006]], when metastability happens,

comparison cycle is elongated compared with the easy comparison with the large input. The entire ADC conversion may not finish within the allocated conversion time. However, if the cycle is too elongated, the ADC fails to convert the input. Incomplete comparison before the clock resets the comparator incurs sparkle codes, which results in non-differential comparator outputs [Chan et al. [2015]]. This happens because comparator does not have enough time to regenerate a valid difference within one asynchronous clock cycle when inputs are small. Since unresolved comparator outputs result in the wrong, non-differential reference voltage selection in capacitive DAC arrays, it can cause larger sparkle codes.

There are several ways to reduce the sparkle code rate. One method is to simply allocate more time for the comparator using the skewed devices in order to wait for the more regenerated outputs [Chen and Brodersen [2006]], but this sacrifices the conversion speed. Another method is to reduce the comparator regeneration time constant, but it has a technology limit and can greatly increase power. To avoid large speed or power penalty, researchers recently developed techniques [Chan et al. [2015]; Keane et al. [2017]; Duan and Alon [2015]]. [Chan et al. [2015]] monitors the differential controls of the DACs by the logic detector and checks whether they are deviated within the conversion cycle. If the non-differential DAC controls are detected, outputs are eventually overridden by the mapped codes. [Keane et al. [2017]] uses an unresolved decision detection scheme with the programmable delay. If an unresolved decision is observed after the prescribed delay, subsequent decisions are ignored. Another technique proposed in [Duan and Alon [2015]] is based on comparator decision time (CDT) quantization.

When metastability happens, the CDT is long. Thus, metastability can be detected by comparing the CDT with a reference delay using an array of 1-bit time-to-digital converters (TDCs). By recording which comparison cycle is in metastability, the correct ADC output can be reproduced, leading to greatly reduced sparkle code rate. Nevertheless, a key limitation of [Duan and Alon [2015]] is that both the CDT and the reference delay are sensitive to process, temperature, and voltage (PVT) variations. Careful foreground hand tuning is used in [Duan and Alon [2015]] to set an appropriate reference delay, but it is unsuitable for practical use and is unreliable in the presence of temperature drift.

This chapter presents a novel sparkle-code reduction technique for high-speed SAR ADCs. It builds upon the basic idea of CDT quantization of [Duan and Alon [2015]], but it ensures PVT robustness by devising a new background calibration technique. Moreover, it makes use of CDT quantization to gain 1-bit increase in the ADC resolution. It works by setting the reference delay $\tau$ to match the CDT when the comparator sees a $\pm 0.25$-LSB input. Background calibration of $\tau$ is enabled by injecting a 0.5-LSB pseudo-random dither to the SAR ADC. If $\tau$ is set correctly, the probability of the comparator seeing an input within $\pm 0.25$ LSB during all SAR conversion cycles is 50%, which is independent of the ADC input because of the injected uncorrelated dither. Thus, by continuously monitoring the rate of TDC outputs being 1, $\tau$ can be background tuned to the desired value. Furthermore, by setting the CDT window to be $\pm 0.25$ LSB, the ADC resolution can be increased by 1-bit by making use of the TDC output, which effectively performs a 0.5-LSB quantization. This means that the proposed architecture can use a 5-bit SAR ADC

to obtain 6-bit. The reduction in the number of comparison cycles increases the ADC speed. In addition, only a 5-bit DAC is needed, leading to a smaller area and faster setting, which also boosts the ADC speed. It is noted that 1-bit resolution increase by using the metastability detector is proposed in [Shikata et al. [2012]]. It also tried to reduce errors originated from the metastability along with the addition of extra resolution. However, its speed is slow and it is still vulnerable to metastability of the detector, which is not adequate for the high-speed ADC.

A prototype ADC equipped with the proposed technique is built in 40nm. The measured sparkle code error is reduced from $10^{-4}$ to below $10^{-9}$. The SNDR is increased from 30.2dB to 35.3dB, which validates the 1-bit resolution enhancement. It samples at 700MS/s and consumes 0.81mW, leading to a Walden figure-of-merit (FoM) of 24fJ/conv-step.

## 2.2 Design of Asynchronous SAR ADC

In order to improve the speed of SAR ADCs, asynchronous clocking has become a popular selection (see Fig. 2.1). In conventional synchronous SAR ADCs, conversion speed is determined by the worst case comparison cycle, which consists of the maximum DAC settling time and CDT. Maximum CDT comes from the minimum resolvable input. Maximum DAC settling time generally happens at MSB or 2nd MSB according to the switching scheme. Asynchronous SAR addresses the fixed allocated time to the comparator [Chen and Brodersen [2006]]. A ready signal ($Rdy$) is generated when the comparison is complete, and it triggers the following comparison. CDT depends on the difference between the input and the ref-

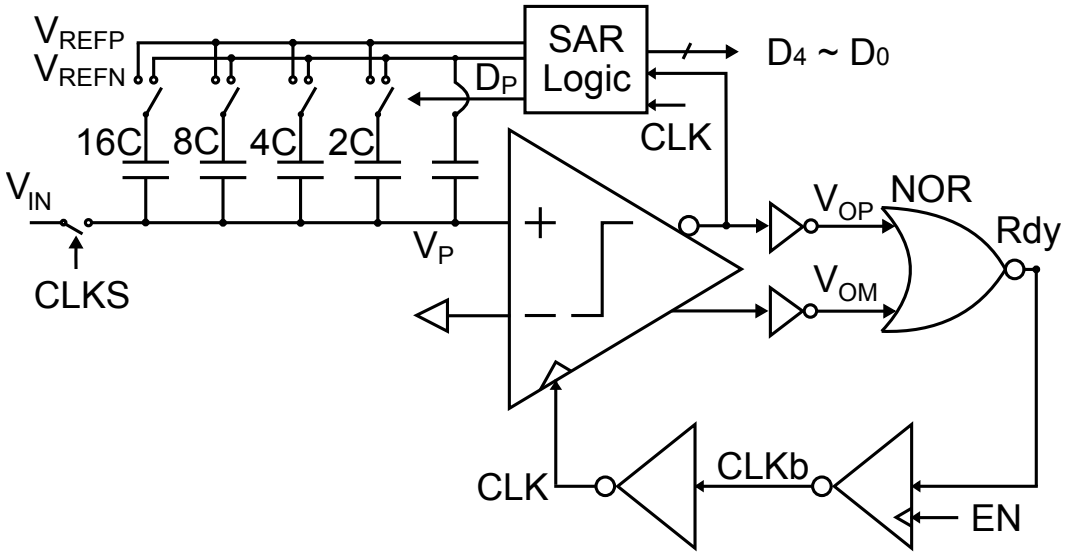


Figure 2.1: Asynchronous SAR ADC.

erence. Since the input falls within $\pm\frac{1}{2}$ LSB at only one conversion cycle in SAR, asynchronous clocking gives the benefit of the shorter total conversion time in comparison with the synchronous counterpart. However, DAC settling time is still the same in [Chen and Brodersen [2006]] as adjustment of the cycle is only about the CDT. Still, the worst case DAC settling time is taken into account to determine the DAC settling time of all cycles. To solve this issue, self-timing technique is tried. For example, [Kapusta et al. [2013]] uses a DAC timer circuit to indicate that DAC settling is finished, which leads to the next comparison cycle in an asynchronous way.

CDT is longest when the input difference is within $\pm\frac{1}{2}$ LSB. The input of the comparator diverges from the reference in the following DAC settling phase in SAR algorithm. In this case, we don't need to wait for the DAC to be settled accurately.

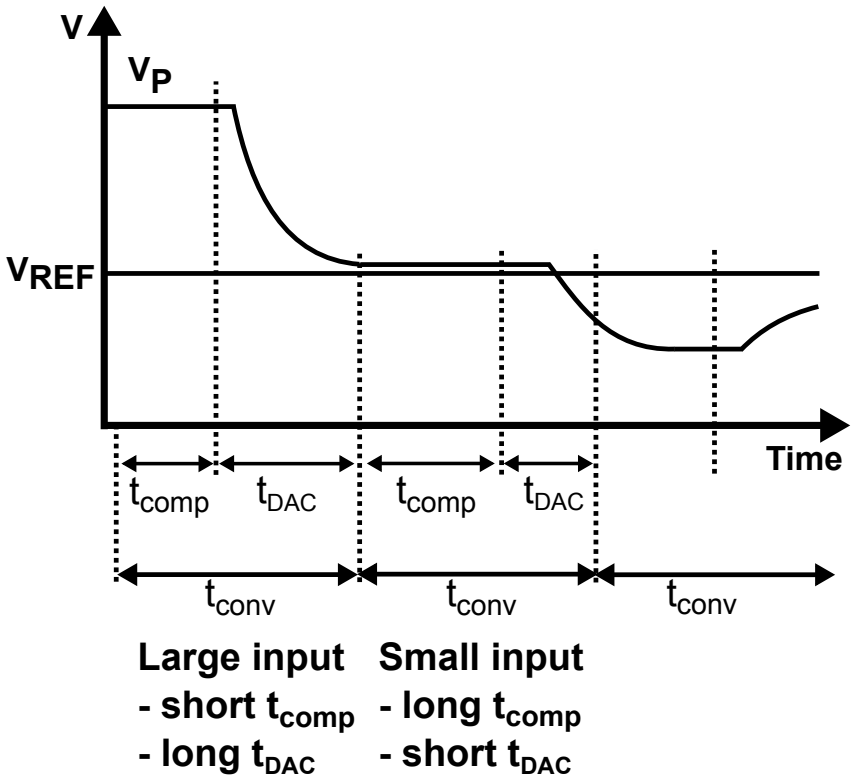


Figure 2.2: Complementary relation between $t_{comp}$ and $t_{DAC}$.

Accurate DAC settling is only required when the input converges to the reference. Under this circumstance, the comparator generates output quickly since the input is not close to the reference. This means that the DAC settling time required is related with the CDT. Generally speaking, from MSB to LSB, the amount of time required by the comparator increases due to the reduced input swing. In contrast, the amount of time that DAC requires for its settling reduces from LSB to MSB. Thus, if we set a fixed time window for comparison and DAC settling, this leads to the most efficient way of using time.

This can be understood in such a way that the comparator can borrow the

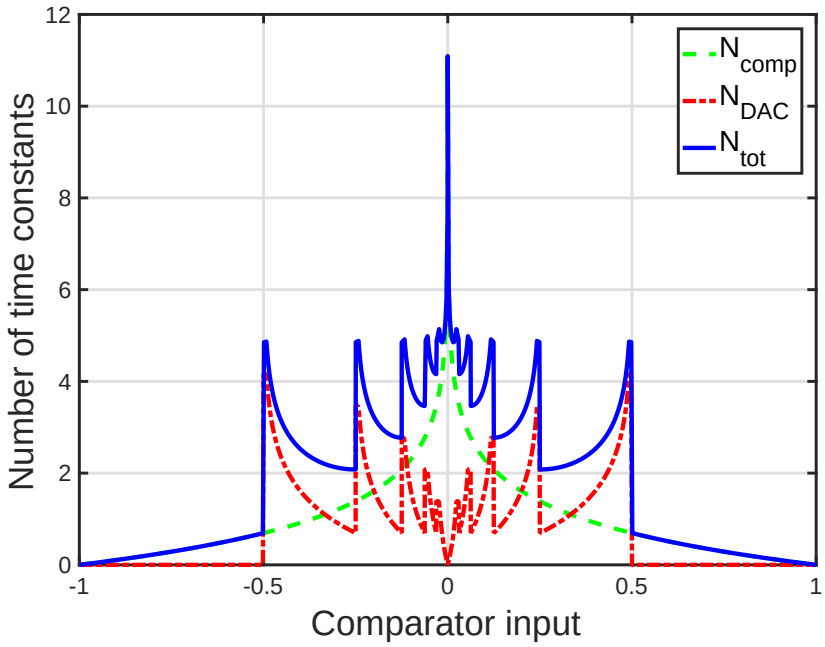


Figure 2.3: $t_{comp}$ and worst-case $t_{DAC}$.

time from the DAC settling if it needs more time to generate the output. Fig. 2.2 illustrates this complementary behavior of the CDT ($t_{comp}$) and DAC settling time ($t_{DAC}$). At the first conversion, the input of the comparator ($V_P$) is large, leading to the short CDT. Subsequent DAC selection moves $V_P$ down toward the reference. Since accurate DAC settling is required, long $t_{DAC}$ is needed. Next comparison shows the opposite case. $t_{comp}$ is long as $V_P$ is close to the reference. It is clear that the DAC voltage is chosen in such a way that $V_P$ diverges from the reference. Therefore, we don't need $V_P$ to be settled for the next comparison. DAC settling continues in the next comparison cycle. Thus, $t_{DAC}$ can be set short. It is noted that the conversion time ($t_{conv}$) for both conversion is the same. Fig. 2.3 shows

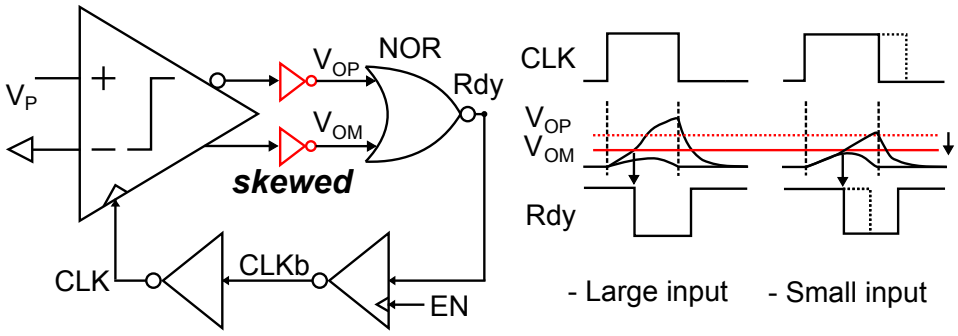


Figure 2.4: Skewed inverters.

the amount of time constant for comparison decision, worst-case DAC settling, and sum of two, respectively in 6-bit SAR simulation with the comparator input range of -1 and 1 and the reference of 0. Note that the amount shown for DAC settling is the worst-case amount at that input. Worst-case DAC settling happens when the input settles to the opposite side with the smallest amplitude. This plot clearly shows the relationship between $t_{comp}$ and worst-case $t_{DAC}$. When $t_{comp}$ is long, $t_{DAC}$ is short and vice versa. Maximum $t_{conv}$ stays constant across the input range except of the input of 0. Therefore, in order to minimize the time wasted during the conversion cycle, the relationship can be applied to the SAR implementation. Also note that a technique dealing with the long CDT (over 5 in this figure) should be required to remove the extremely long $t_{comp}$ due to the metastability at 0 input.

In order to build up this scheme, time of one conversion should not depend on CDT. This can be implemented by making the comparator faster by employing the skewed inverters (in Fig. 2.1) instead of making the comparator waiting for resolved comparator outputs as in Fig. 2.4. In the beginning, comparator outputs ($V_{OP}$, $V_{OM}$) stay at the same reset low voltage. After comparison starts, outputs

start to resolve. $V_{OP}$ and $V_{OM}$ increase together until the regeneration phase. If that increase is detected by NOR instead of waiting for the fully resolved outputs, it forces the ADC to proceed to reset the comparator after the prescribed delay which is defined by the clock generation loop. In Fig. 2.4, even with the small input, $Rdy$ goes down before $V_{OP}$ and $V_{OM}$ resolve to the differential values due to the lowered threshold. With the oppositely-skewed inverters, $Rdy$ is generated later with a big dependence on the input as illustrated in the dashed line. As mentioned, unsettled DAC does not affect the next comparison. Reset time is adjusted by the comparison time since large input leads to the quick resolved outputs, resulting in the steeper change of $Rdy$. In this simple implementation, $t_{conv}$ is not perfectly constant. However, by using the skewed inverters, the dependence on the input can be reduced. This means that within relatively constant cycle, $t_{comp}$ and $t_{DAC}$ is self-adjusted according to the input without any external logic or timer. However, if CDT is too long due to the metastability as in Fig. 2.3, the ADC may fail to create the correct DAC voltages since the comparator is reset after a certain time regardless. Therefore, the way to detect the long CDT is needed to remove the errors.

## 2.3 Sparkle Code Error

### 2.3.1 Cause of Sparkle Code Error

As the speed continues to increase, less time is available for the comparator decision leading to the metastability. Since outputs regenerate exponentially with time, if the input is very close to the reference, the comparator takes a much

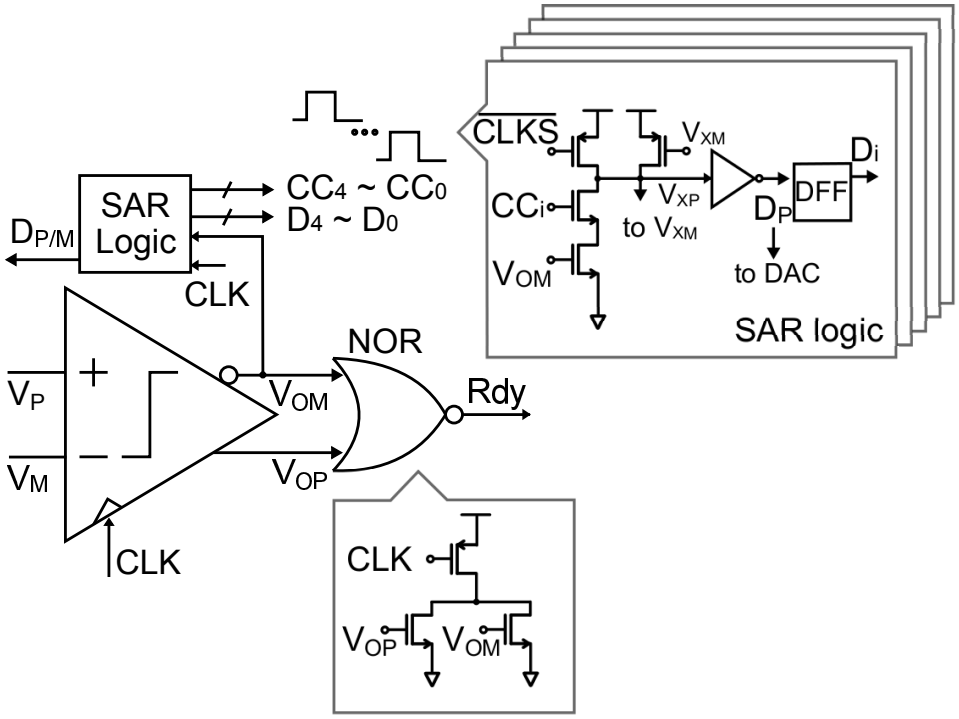


Figure 2.5: Asynchronous SAR ADC with dynamic logic gates

longer time for a valid logic output within the allowable comparison time. Therefore, elongated CDT causes the ADC not to finish within the allocated conversion time. This results in the non-differential outputs of the SAR logic and DAC arrays. Fig. 2.5 shows the comparator with SAR logic and NOR. Dynamic NOR is employed to make the clock generation loop faster because of the less stacked transistors. Not like the static NOR, it raises the ready signal even before the outputs are fully resolved. SAR logic also utilizes the dynamic logic with precharging, selection and latch functions. Note that a keeper transistor is placed at $V_{XP}$ node to push the differential transition quicker in the dynamic logic pair. As mentioned, with a small input, a comparator does not have enough time to regenerate results

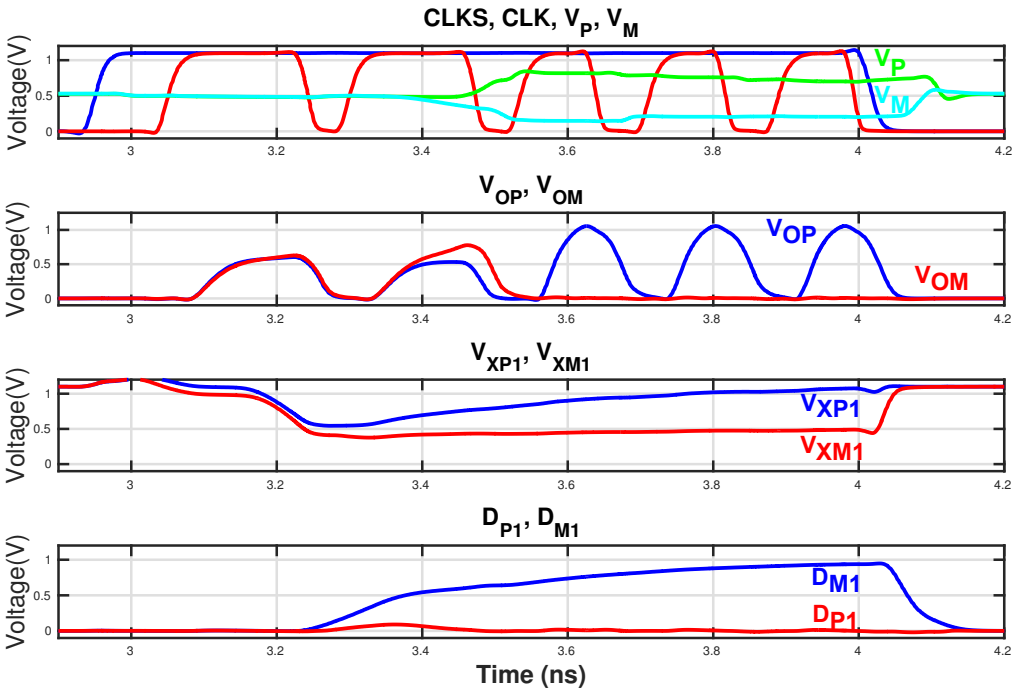


Figure 2.6: Sim. of the metastabiltiy-induced error

before the corresponding comparison cycle ($CC$ in Fig. 2.5) turns off the middle transistor in the logic. This entails non-differential voltages at the node $V_{XP}$ and $V_{XM}$, consequently producing non-differential DAC control voltages. In the worst case, DAC control voltages do not change after the conversion, which leaves the input voltage the same. Then the same metastability issue is again encountered in the next comparison.

Fig. 2.6 illustrates this type of error in the worst-case simulation with the input same as the reference. Subscript 1 means the first cycle. As can be seen in the plot, at the end of the first comparison cycle, comparator outputs $V_{OP}$ and $V_{OM}$ cannot generate the valid logic outputs. Due to the dynamic NOR, even unresolved

outputs raise the ready signal, which reset the comparator. As a result, $V_{XP1}$ and $V_{XM1}$ are not in the differential state. Owing to the keeper transistors, voltages keep changing slowly. Note that DAC voltage $V_{M1}$ increases even after the first cycle, which causes the input of the comparator to change on. This contributes to the large sparkle code errors. This concludes that schemes to avoid the metastability-induced errors are required, especially in the high-speed SAR design with less available comparison time.

### 2.3.2 Sparkle Code Removal Tachniques

Simple technique is to allocate more time to the comparator using the skewed devices at the last inverter stage of the comparator to effectively make the CDT long because the clock depends on CDT, therefore reset time is delayed. However, this sacrifices the conversion speed even in normal condition. Simulation shows that speed can be slower by 20% or more. Another way to use the latched output ($D_P$ and $D_M$ in Fig. 2.5) instead of comparator outputs ($V_{OP}$ and $V_{OM}$ in Fig. 2.5) for the inputs of NOR. This slows down clock generation. Since comparison cycle ($CC$ in Fig. 2.5) also depends on the clock cycle, more time is allowed for the comparison. Disadvantage is that time to go through the dynamic logic gate is wasted regardless of the metastability. This concludes that detection of the metastability-induced errors and replacement of outputs [Chan et al. [2015]; Keane et al. [2017]] is better than the artificial CDT elongation. As mentioned earlier, CDT quantization technique is proposed by [Duan and Alon [2015]]. Fig. 2.7 shows how CDT quantization works. $V_{OP}$ and $V_{OM}$ are reset to high before comparison. After $CLK$

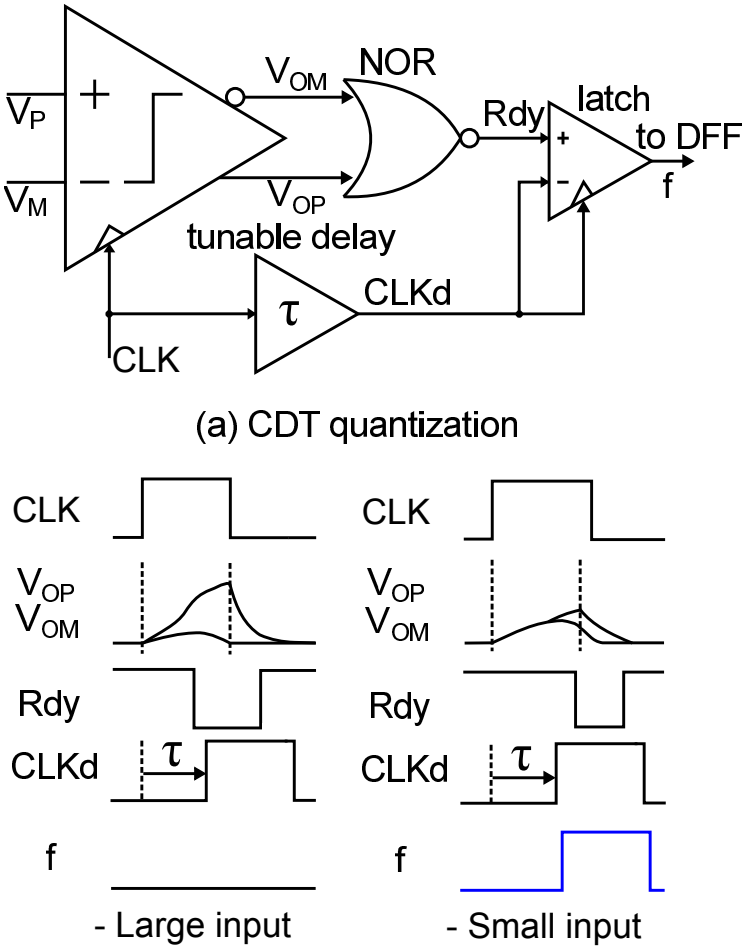


Figure 2.7: CDT quantization

fires, a latch detects the output of NOR ($Rdy$) after $\tau$ delay. When the input difference between $V_P$ and $V_M$ is small, metastability happens. Therefore, the CDT is long. Thus, ready goes down later than $\tau$. In result, the latch catches high to tell that the metastability happens. This process can be seen as comparison of CDT with a reference delay using an array of 1-bit time-to-digital converters (TDCs). By

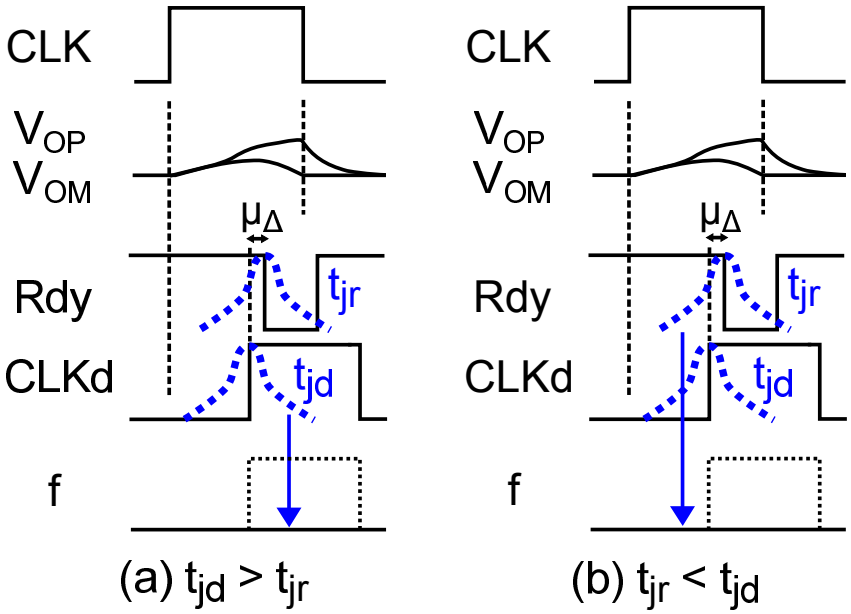


Figure 2.8: False negative detection error

recording which comparison cycle is in metastability, the correct ADC output can be reproduced as in [Chan et al. [2015]].

### 2.3.3 Metastability Detection Error Analysis

There are two types of errors in the proposed metastability detection techniques [Duan and Alon [2015]]. One is false positive error, which means that metastability is detected by the detector, but actually the comparator is not in metastability. This error happens when the residue is very close to the detection window, therefore, only to increase the noise. The other is false negative error, which is that although hard metastability happens, it is not detected. This is primarily due to the normally distributed instantaneous jitter of the tunable delay and the signal path.

Fig. 2.8 illustrates the jitter-induced detection errors. $t_{jd}$ represents an arrival time of $CLKd$ with a jitter of having a normal distribution with the mean of $\mu_{CLKd}$ and the variance of $\sigma^2_{CLKd}$. $t_{jr}$ is an arrival time of $Rdy$ with a normally distributed jitter with the mean of $\mu_{Rdy}$ and the variance of $\sigma^2_{Rdy}$. False negative error occurs when $CLKd$ comes later than Rdy due to the jitters as shown in Fig. 2.8(a). It also happens when $Rdy$ falls earlier than $CLKd$ going up due to the jitters as illustrated in Fig. 2.8(b). Since $t_{jd}$ and $t_{jr}$ are independent, the difference of $t_{jd}$ and $t_{jr}$ is also a normal distribution with the mean of $\mu_\Delta = \mu_{CLKd} - \mu_{Rdy}$ and the variance of $\sigma^2_\Delta = \sigma^2_{CLKd} + \sigma^2_{Rdy}$. As the probability of Fig. 2.8(a), $P(t_{jd} > t_{jr})$, is equivalent to $P(t_{jd} - t_{jr} > 0)$, the probability of the false negative error can be calculated by the Q-function (Eq. 2.1) of the difference of the two normal distributions.

$$\begin{aligned} \mathrm{Q(x)} &= \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp(-\frac{u^2}{2})\mathrm{d}u \qquad (x = \frac{\mu_\Delta}{\sigma_\Delta}) \\ &= \frac{1}{2}[1 - \mathrm{erf}(\frac{x}{\sqrt{2}})] \end{aligned} \tag{2.1}$$

where erf means the error function. For Fig. 2.8(b), similar calculation can be performed by using $P(t_{jr} < t_{jd}) = P(t_{jr} - t_{jd} < 0)$ with the mean of $\mu_{Rdy} - \mu_{CLKd}$. Fig. 2.9 shows the calculation of the false negative detection error rate according to the $\mu_\Delta$ which is normalized to $\sigma_\Delta$. Standard deviations of $t_{jr}$ and $t_{jd}$ are $0.17\tau_{comp}$ and $0.20\tau_{comp}$, respectively, which are obtained from the simulation. $\tau_{comp}$ is the comparator regeneration time. As mentioned, sparkle code occurs when the compactor cannot regenerate the outputs with the small input within the elongated comparison time before the comparator reset. In the proposed SAR ADC,

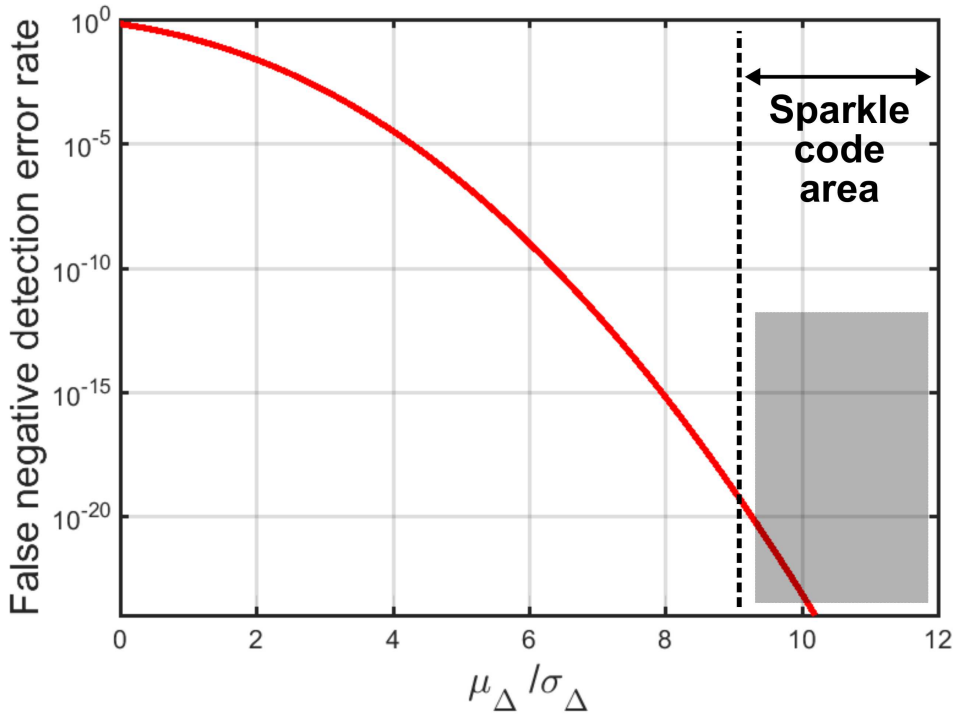


Figure 2.9: Calculation of false negative detection error rate

that elongation corresponds to the more than $9 \sim 10$ times $\sigma_\Delta$, where the false negative error rate is very low as shown in the shaded area in Fig. 2.9.

## 2.4 Proposed ADC Design

### 2.4.1 Design of the 5-b Asynchronous SAR ADC Core

Fig. 2.10 shows the schematic of the single-ended version of the proposed ADC. Its core is a 5-bit SAR with asynchronous clock generation [Chen and Brodersen [2006]]. After sampling, $EN$ turns high and starts the first comparison [Fig. 2.11(a) shows the timing diagram]. NOR detects when the comparison finishes. After two

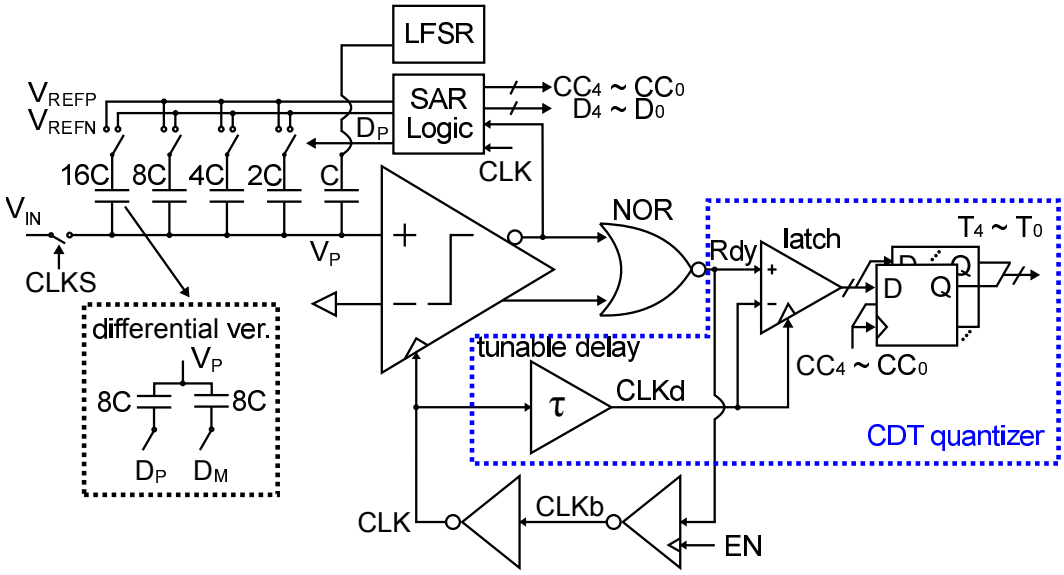


Figure 2.10: Architecture of the proposed SAR ADC.

inverter delay, it triggers the comparator reset, and then, initiates the next comparison. The SAR logic counts the comparison cycle [$CC_i$ being 1 indicates the $(5-i)$-th comparison cycle] and records the comparator outputs ($D_4 \sim D_0$) using dynamic logic circuits to increase speed and save power. The DAC switching scheme of [Liu et al. [2010]] is adopted to reduce DAC switching power. By splitting capacitors in half, it effectively realizes $V_{cm}$-based switching but without the need to connect capacitors to $V_{cm}$, which would require a large switch size.

### 2.4.2 CDT Quantization and Sparkle Code Removal

The CDT quantization block is shown in the dashed blue box of Fig. 2.10. The dynamic latch works as a 1-bit TDC that compares the CDT with a reference

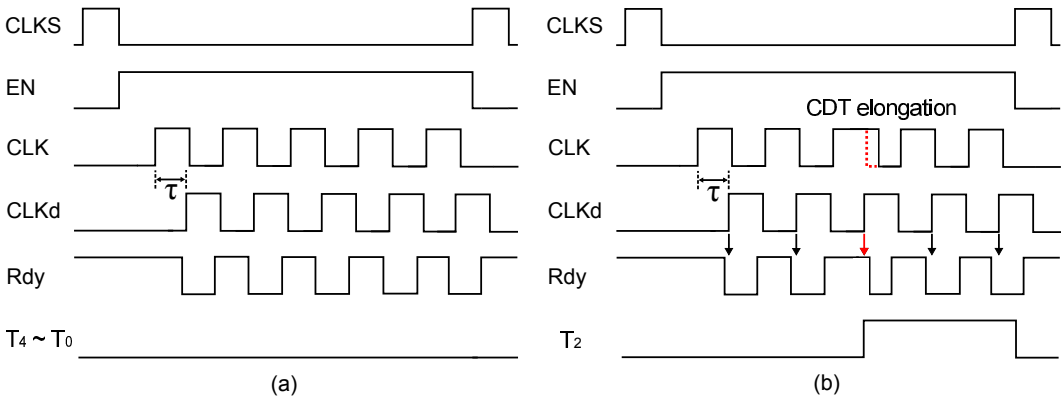


Figure 2.11: Waveform: (a) normal operation; (b) metastability in the 3rd comparison

delay $\tau$. The latch is triggered after every comparison. Its output is stored in an array of DFFs ($T_4 \sim T_0$) according to the comparison cycle $CC_i$. This way, when comparator metastability happens, we will not only detect it but also know when it happens.

Fig. 2.11(b) shows an example timing diagram when the 3rd comparison has a long CDT. In this case, the NOR output $Rdy$ arrives later than the delayed clock $CLKd$, leading to $T_2 = 1$. However, the error can be corrected because we know the comparator input is very close to zero during the 3rd comparison based on $T_2 = 1$, and thus, we can directly obtain the correct ADC output based on $D_4$ and $D_3$. We do not even need to know $D_2 \sim D_0$. In other words, when we see $T_i = 1$, we can directly assign $D_i \sim D_0$. Table 2.1 summarizes how the ADC output is corrected for any comparison cycle with a long CDT. For $T_2 = 1$, $\overline{D_4 D_3 D_2 D_1 D_0}$ is replaced by $\overline{D_4 D_3 011}$.

Table 2.1: Mapping from the raw ADC output to the corrected output.

| | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $T$ |
|---|---|---|---|---|---|---|
| $T_4 = 1$ | 0 | 1 | 1 | 1 | 1 | 1 |
| $T_3 = 1$ | $D_4$ | 0 | 1 | 1 | 1 | 1 |
| $T_2 = 1$ | $D_4$ | $D_3$ | 0 | 1 | 1 | 1 |
| $T_1 = 1$ | $D_4$ | $D_3$ | $D_2$ | 0 | 1 | 1 |
| $T_0 = 1$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | 0 | 1 |

### 2.4.3 Choice of $\tau$ and 1-bit Resolution Enhancement

The value of the reference delay $\tau$ needs to be set very carefully. Let us define the value of the comparator input that produces an equal delay of $\tau$ as $W$, where $W$ is inversely proportional to $\tau$. The TDC can be considered as a window detector. It detects comparator input that falls inside $[-W, +W]$. When the comparator input is within $\pm W$, the TDC output is 1, otherwise, the TDC output is 0. $W$ needs to be set properly. It cannot be larger than 1 LSB, as otherwise, even when the comparator is in normal operation with an input greater than 1 LSB, it would be identified as being in metastability, causing ADC resolution degradation. $W$ also cannot be too small, as otherwise, a long CDT may not be detected by the TDC, leaving some sparkle codes uncorrected.

We choose the value of $\tau$ such that its corresponding $W$ is 0.25 LSB. In other words, if the comparator input is within $\pm 0.25$ LSB, its CDT is longer than $\tau$ and the TDC output will be 1. Choosing $W = 0.25$ LSB ensures that all sparkle codes due to metastability are identified. More importantly, it enables 1-bit increase in the ADC resolution. Fig. 2.12 compares three cases of $W$. The black vertical

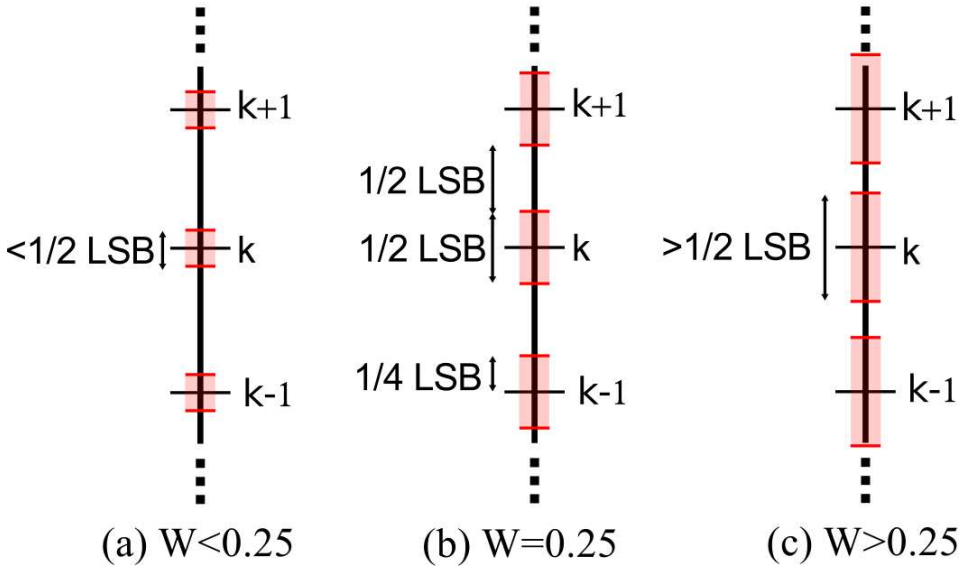


Figure 2.12: Choice of the window width $W(\tau)$.

line indicates the ADC input/output ranging from 0 LSB to 31 LSB for the 5-bit SAR ($k$ marks the location of $k$ LSB). The red shaded part indicates the region over which one TDC output $T_i$ is 1. It is clear that if $W = 0.25$ LSB, the shaded and unshaded regions evenly divide up the ADC input range. This indicates that one extra bit can be obtained by making use of $T_i$. If we define $T = T_4||T_3||T_2||T_1||T_0$ ($T = 1$ when any $T_i$ is 1), then $T$ provides a 0.5-LSB quantization and can be directly concatenated with the corrected 5-bit ADC output $\overline{D_4D_3D_2D_1D_0}$ to obtain a 6-bit ADC output, as $\overline{D_4D_3D_2D_1D_0T}$. This is also shown in Table 2.1. $T$ is now the new LSB of the 6-bit ADC: $T = 1$ when the input is in the red shaped regions, and $T = 0$ otherwise.

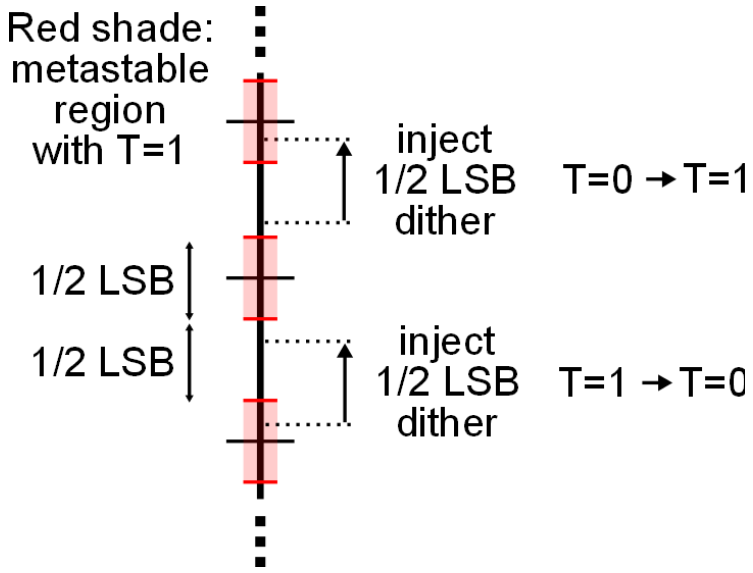


Figure 2.13: Dither based background calibration of window width $W$.

### 2.4.4 Background Calibration of the Reference Delay $\tau$

Since the window width $W$ is set by the delay $\tau$, $\tau$ needs to be controlled very accurately. Nevertheless, this is nontrivial because delay is sensitive to PVT variations. Foreground calibration was used in [Duan and Alon [2015]] to manually tune $\tau$, but this is not suitable for practical application and cannot ensure robustness when voltage or temperature drifts. Background calibration is necessary to ensure PVT robustness.

We propose a novel background calibration technique that ensures $W = 0.25$ LSB. The key idea is based on monitoring the probability of $T = 1$. As shown in Fig. 2.12, as $W$ increases, the red shaded region enlarges, and thus, there is a higher probability of $T = 1$ assuming a random input. Hence, by monitoring $P(T = 1)$ and adjusting $\tau$ to keep $P(T = 1) = 50\%$, we can ensure that $W =$

$0.25$ LSB across PVT variation. The relation between $P(T = 1)$ and resolution improvement is as follows [Shikata et al. [2012]]. From this Eq. 2.2 ($P(T = 1)$ is abbreviated as P), if $P(T = 1) = 50\%$, which means $W = 0.25$ LSB, then SNR improvement is 6 dB.

$$\Delta SNR = -10 \times \log(1 - 3P + 3P^2) \qquad (P < 1) \tag{2.2}$$

This background calibration scheme works well for a busy ADC input. However, if the ADC input is a fixed DC value, the measured $P(T = 1)$ becomes strongly input-dependent and no longer correlates well with $W$. For example, if the DC input is right at the center of a red shaded region of Fig. 2.12(b), $P(T = 1) = 100\%$ even though $W = 0.25$ LSB. This can cause $\tau$ to be incorrectly adjusted. To increase the robustness of the proposed background calibration technique, we inject a 0.5-LSB pseudo-random dither into the SAR ADC after the sampling phase as shown in Fig. 2.11. The dither is produced on-chip using a linear feedback shift register (LFSR). The addition of the dither, together with the inherent ADC noise, makes $P(T = 1)$ independent from the ADC input. As shown in Fig. 2.13, if an input falls into a $T = 1$ region, adding a dither pushes it into a region with $T = 0$, and vice versa. This way, to the first order, $P(T = 1)$ does not depend on the input anymore; it depends only on the window width $W$. It is noted that if there is no inherent noise, at certain DC, even with the window width of Fig. 2.12(a) or (c), the $P(T = 1)$ can be $50\%$. Inherent noise such as $KT/C$ helps to relieve this limitation. Simulation shows that noise with the sigma of 0.1 $\sim$ 0.2 LSB is needed for this purpose. Thus, capacitive size and comparator are

designed to meet the above requirement. As a result, the proposed background calibration technique with dither can work for any type of ADC input regardless of its amplitude, frequency, or distribution.

### 2.4.5 Circuit Implementation

The schematic of a comparator, a latch and a tunable delay used in the CDT quantizer is shown in Fig. 2.14. A 3-stage comparator shown in Fig. 2.14(a) is used for speed consideration, since it is two times faster than the 2-stage counterpart. Double-tail comparator [Shinkel et al. [2007]] utilizes both $CLK$ and $CLKb$ by placing PMOS instead of NMOS in the latching stage. This PMOS loads the $CLKb$ node of the asynchronous clock generation path. Inverters in the comparator are skewed to have the strong PMOS. Thus, once the conversion starts and $V_{P2}$/$V_{M2}$ decrease in the beginning, $OUTP$/$OUTM$ rise together up to the regeneration point. Since the dynamic NOR is used, the ready signal is raised even though outputs are not fully differential. Furthermore, PMOS size is larger than NMOS for the same strength, thus it further slows the asynchronous clocking.

Fig. 2.14(b) is the schematic of the latch in the CDT quantizer. As $CLKd$ and $\overline{Rdy}$ are both zero at sampling, a current tail transistor is removed for the fast latching since less number of transistors are stacked without the tail NMOS transistor. Dynamic latch is placed prior to DFFs because DFF is slow to catch data before the comparator is reseted. Tunable delay is shown in Fig. 2.14(c). Current-controlled NMOS is inserted at the bottom of the first inverter. 3 inverters with the appropriate size are followed. Delay can be tuned from 40ps to 100ps.

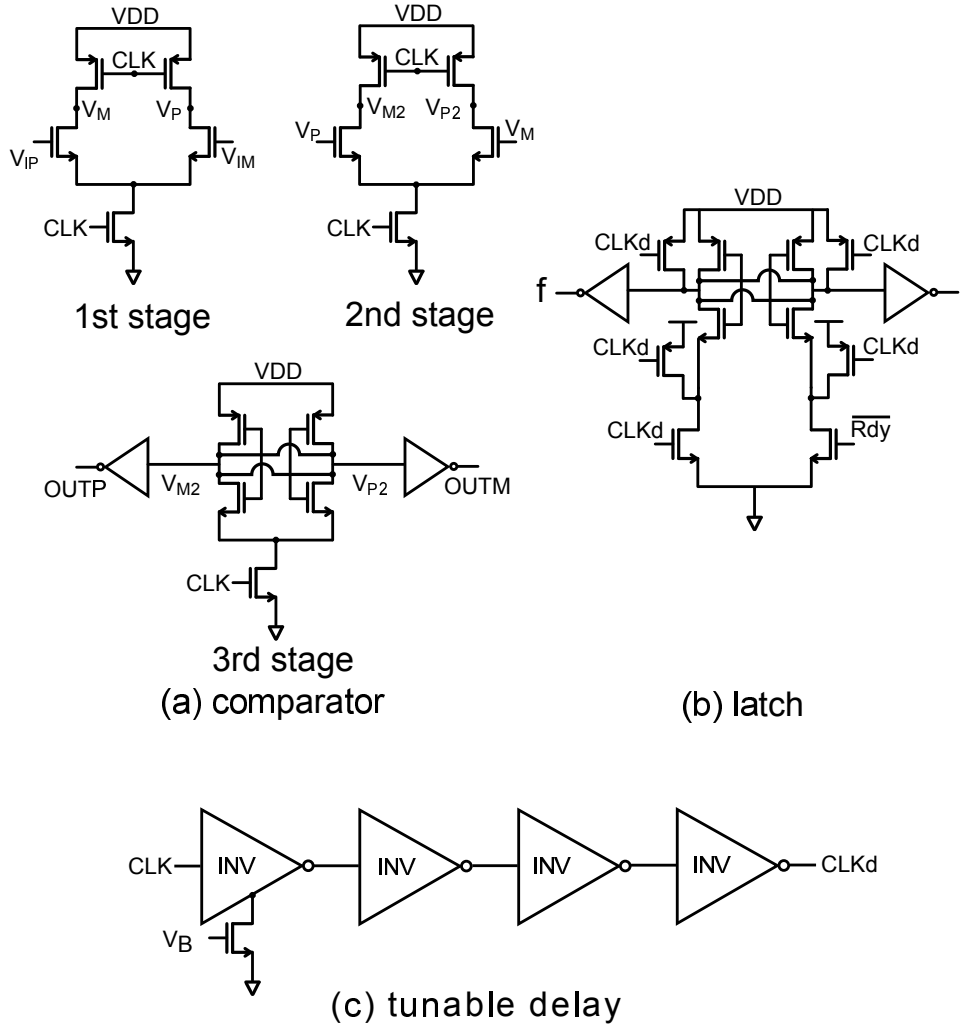


Figure 2.14: Schematic of (a) comparator, (b) latch, and (c) tunable delay

## 2.5 Measurements

The prototype ADC in 40nm LP CMOS occupies 0.003mm$^2$ (see Fig. 2.15 for die photo). The unit DAC capacitor is 0.25fF. Fig. 2.16 shows two example measured ADC outputs with sparkle codes. With the proposed technique, these sparkle codes are detected and corrected using Table 2.1.

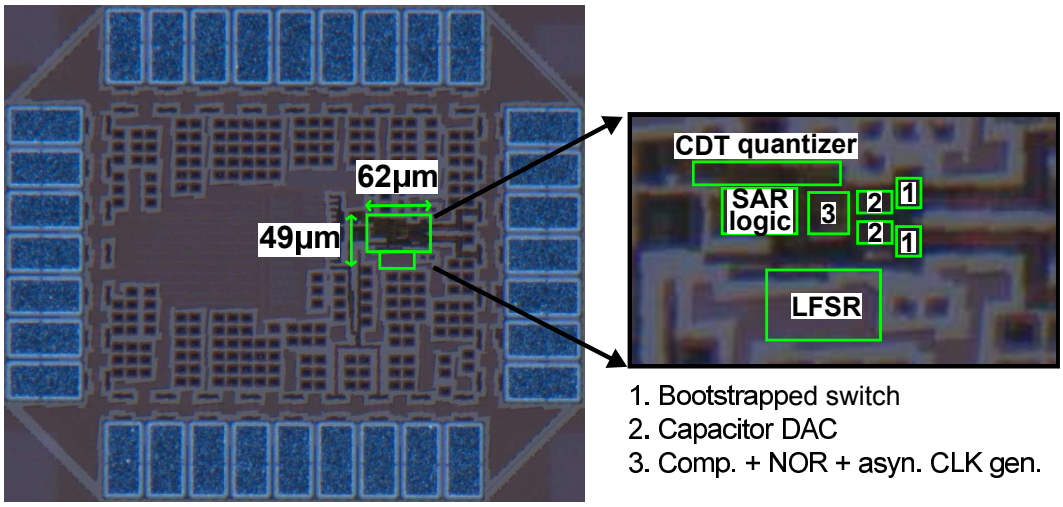


Figure 2.15: Chip die photo.

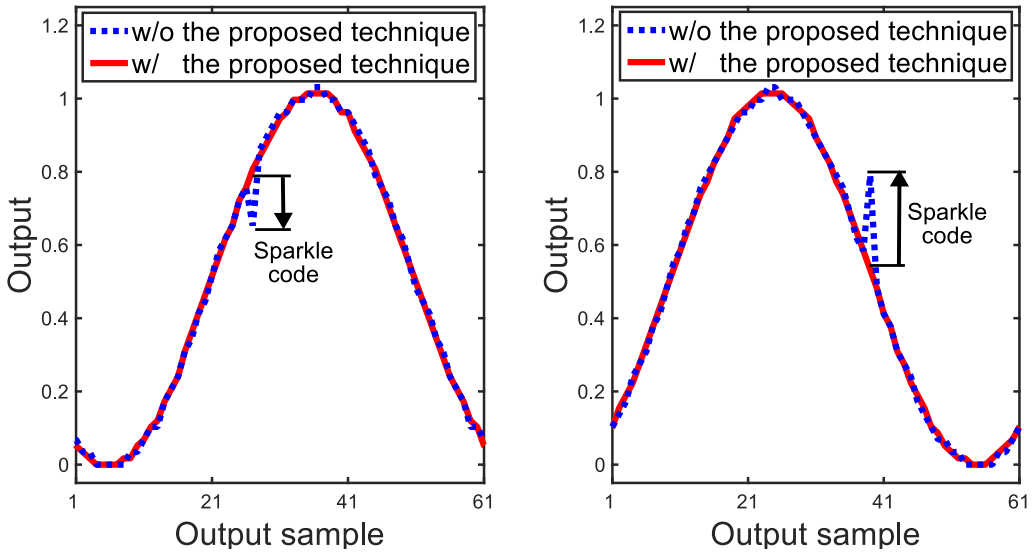


Figure 2.16: Measured ADC output waveform with sparkle codes.

Since ADC thermal noise can also cause small bit flips, we define the detection of a sparkle code event only when the ADC error is greater than 4 LSB

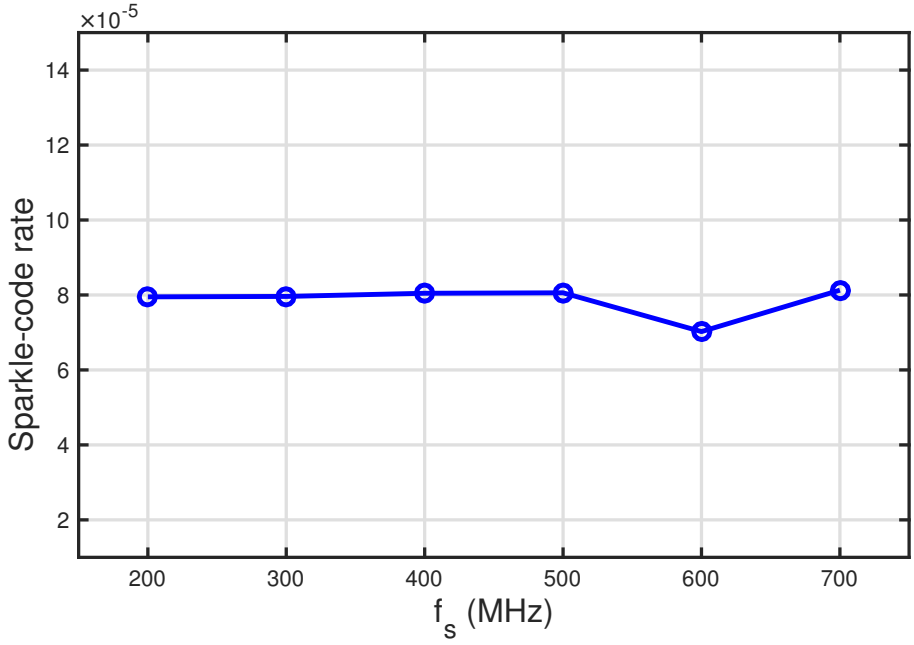


Figure 2.17: Measured sparkle code rate vs. sampling frequency

(using the 6-bit scale). The measured sparkle-code occurrence is $1.9 \times 10^5$ out of $2 \times 10^9$ samples, leading to an error rate of $10^{-4}$. Sparkle code rate according to the sampling frequency is measured and plotted in Fig. 2.17. Sparkle code rate remains almost similar across the sampling frequency from 200MHz to 700MHz under the same input frequency. This shows that major mechanism of the sparkle code is the non-differential outputs of the comparator. If the elongated conversion time is the cause, sparkle code rate should be in decrease as the sampling frequency is reduced. With the proposed sparkle code reduction technique, we cannot measure any sparkle code, which indicates that the proposed technique has suppressed the sparkle code rate to be below $5 \times 10^{-10}$.

Fig. 2.18 shows the histogram of the measured locations of the sparkle

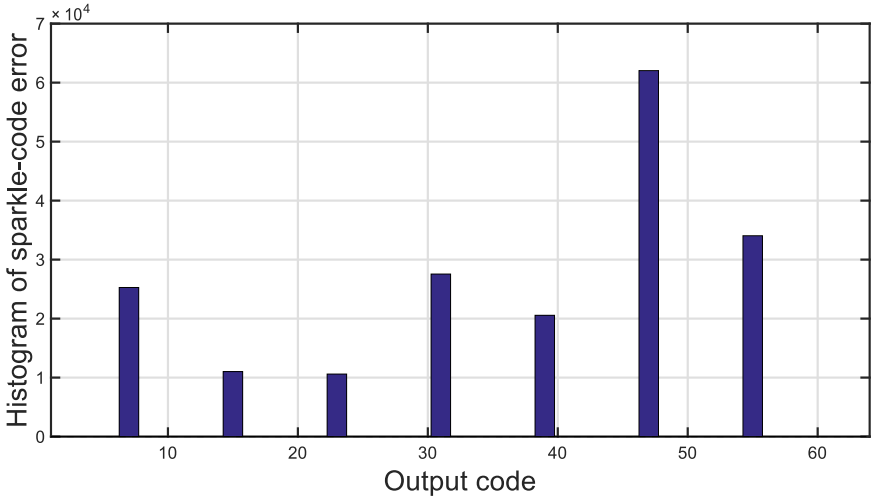


Figure 2.18: Histogram of the location of the sparkle codes

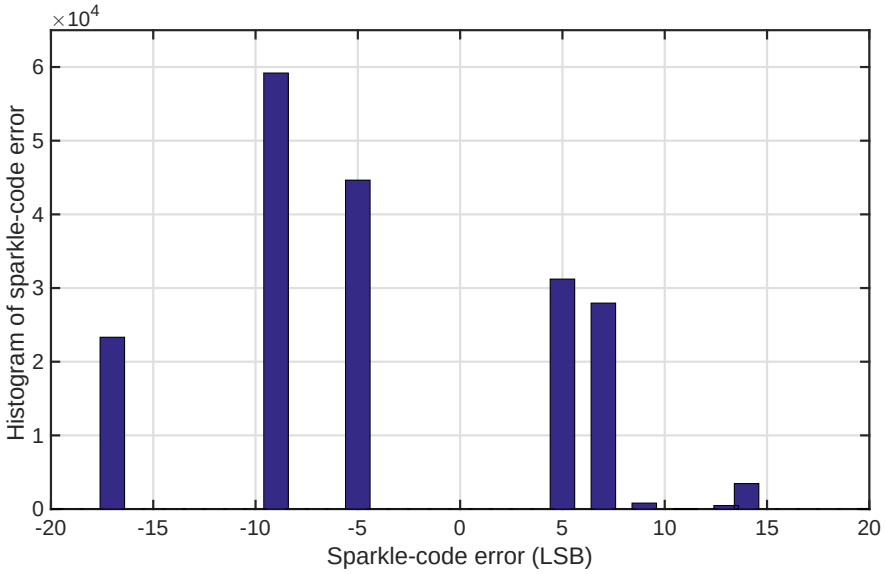


Figure 2.19: Histogram of the magnitude of the sparkle codes

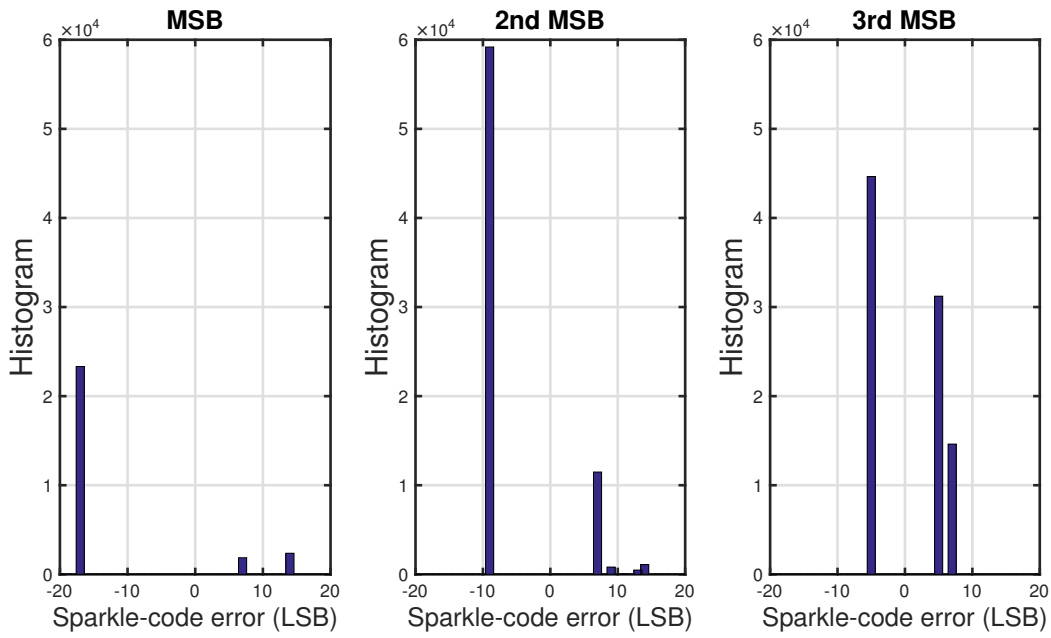


Figure 2.20: Histogram of MSB, 2nd MSB and 3rd MSB sparkle codes

codes. As expected, since metastability can happen during any comparison cycle, sparkle codes show up at all major MSB transitions. We have also measured the magnitude of the sparkle code errors. Fig. 2.19 is the histogram of the measured sparkle code error. The largest error is 17 LSB. The mean and standard deviation are 8.2 and 3.9 LSB, respectively. Reason for the unequal distribution of the above histograms are thought to be the unsymmetrical parasitic capacitance along the differential paths. Fig. 2.20 shows three histograms corresponding to the first 3 MSBs. These plots show that most of the largest errors occur at MSB conversion. The total number of sparkle code error is in increase from the 1st to the 3rd MSB as expected. The reason why big sparkle code error occur is that combination of the non-differential DAC voltages after the cycle and the slow change thereafter as can

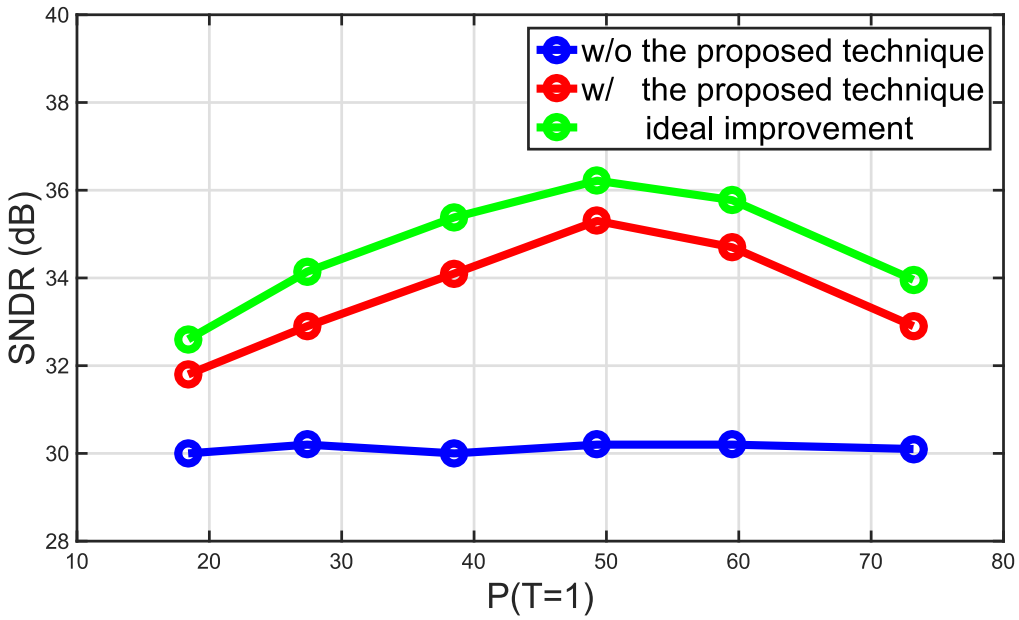


Figure 2.21: SNDR versus the probability of $T = 1$.

be seen Fig. 2.6. This causes the input voltage of the comparator keep changing after the corresponding cycle, which results in the wrong residue voltage.

The measured resolution improvement using the proposed technique versus $P(T = 1)$ is shown in Fig. 2.21. As expected, $P(T = 1) = 50\%$ leads to the largest SNDR improvement. The green curve indicates the theoretical upper limit for the resolution improvement from the equation 2.2. The measured result follows it. There is a small 1-dB difference, which is due to ADC noise and capacitor mismatch that are not considered in the theoretical calculation. The measurement result of Fig. 2.21 also validates the proposed background calibration technique: by adjusting the delay $\tau$ and keeping $P(T = 1) = 50\%$ in the background, we can ensure robust operation across PVT variation. Since the estimation of $P(T = 1)$

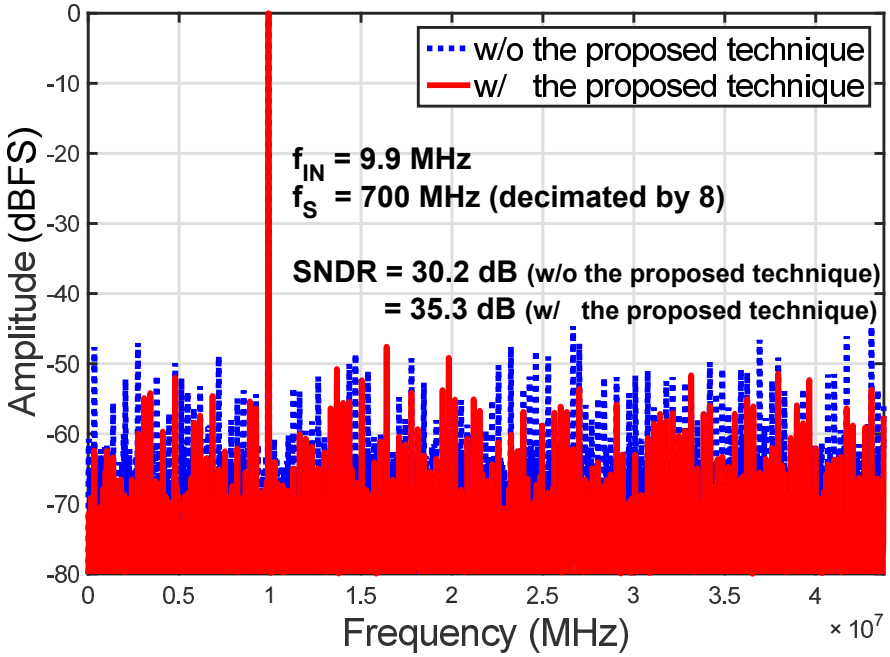


Figure 2.22: Measured ADC spectrum ($2^{13}$ points)

is fast, the convergence time of the proposed background calibration technique is short. Measurement shows that $10^5$ samples or 0.2ms is sufficient.

Fig. 2.22 shows the measured ADC spectrum. The sampling rate is 700MS/s and the output is decimated by 8 to simplify testing. The measured SNDR of the 5-bit ADC core is 30.2 dB. It increases to 35.3 dB with the proposed resolution enhancement technique. The measured SNDR versus input amplitude and frequency are shown in Fig. 2.23. Consistent SNDR improvement is obtained. Measured INL and DNL are $+0.9/-0.1$ and $+0.5/-0.4$ LSB, respectively (in Fig. 2.24), limited by capacitor mismatch.

The measured total ADC power is 0.81mW. The analog power consumed

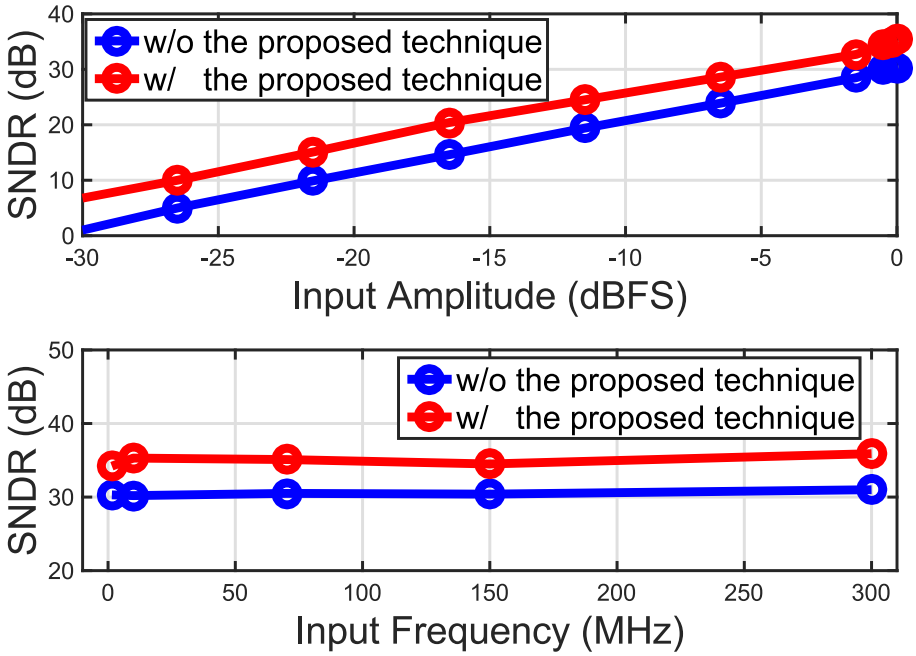


Figure 2.23: SNDR vs. input amplitude and frequency

by comparator, asynchronous clock generation, and CDT quantizer is 0.4mW. The reference power is 0.07mW. The digital power consumed by SAR logic and LFSR is 0.34mW, Table 2.2 compares this work with other works. The measured Walden FoM is 24.4 fJ/conv-step, which is in-line with the state-of-the-art.

## 2.6 Conclusion

This chapter presented a sparkle-code correction technique for high-speed single-channel SAR ADCs. It can reduce the sparkle code error rate by more than 4 orders of magnitude. Moreover, it can increase 1-bit ADC resolution by setting the metastability detection window to be 0.25 LSB. The robustness of the pro-

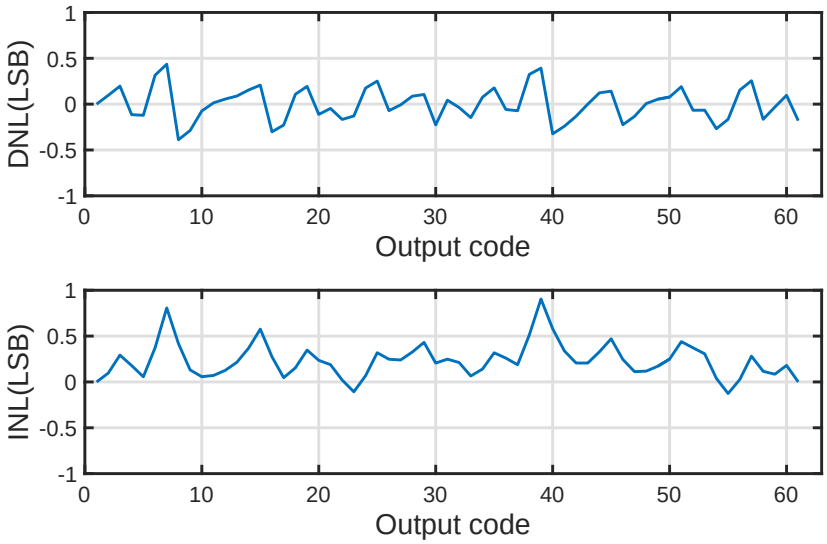


Figure 2.24: DNL and INL plots

Table 2.2: Comparison with state-of-the-art 6b high-speed SAR ADCs

| | This work | Duan and Alon [2015] | Choo et al. [2007] | Jiang et al. [2012] |
|---|---|---|---|---|
| Feature | | | | |
| Sparkle-code reduction | O | O | X | X |
| 1-bit resolution enhancement | O | X | X | X |
| Background calibration | O | X | - | - |
| Chip performance | | | | |
| Technology (nm) | 40 LP | 28 SOI | 40 | 40 |
| Type | SAR | TI SAR | ciSAR | SAR |
| Sample rate (GS/s) | 0.7 | 0.64* | 1 | 1.25 |
| Bits | 6 | 6 | 6 | 6 |
| SNDR (dB) | 35.3 | 25.2 | 34.6 | 31.8 |
| ENOB | 5.57 | 3.89 | 5.46 | 4.99 |
| Power (mW) | 0.81 | 5.3* | 1.26 | 7.26 |
| Area ($mm^2$) | 0.0031 | 0.14 | 0.00058 | 0.014 |
| FOM (fJ/conv-step) | 24.4 | 555 | 28.7 | 183 |
| *single-channel performance | | | | |

posed technique is ensured by a novel dither based background calibration technique based on probability measurement.

# Chapter 3

# VCO-Based Continuous-Time $\Delta\Sigma$ ADC

## 3.1 Modular Architecture and DAC Calibration

The first section[1] of this chapter presents a low-power and small-area VCO-based closed-loop $\Delta\Sigma$ ADC with two highlights. First, the ADC has a distributed modular architecture. It consists of repetitive slices, which simplifies both schematic and layout design. It allows the ADC to be easily reconfigured for other resolution specifications. Second, a novel digital DAC mismatch calibration technique is proposed. It has low hardware complexity by taking advantage of the intrinsic clocked averaging (CLA) capability of dual VCO-based integrator. It ensures high linearity in the presence of large DAC mismatches. A prototype ADC in 130nm CMOS occupies only 0.04mm$^2$. It achieves 71dB SNDR over 1.7MHz BW while sampling at 250MS/s and consuming 0.9mW under a 1.2V supply.

This section is organized as follows: an introduction is first presented. The schematic and layout design of the proposed VCO-based $\Delta\Sigma$ ADC are explained next. Explanation of the proposed digital DAC mismatch calibration technique is

[1]This section is a reprint of the publication: Yeonam Yoon, Kyoungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen and Nan Sun, "A 0.04-$mm^2$ Modular $\Delta\Sigma$ ADC with VCO-based Integrator and 0.9-mW 71-dB SNDR Distributed Digital DAC Calibration", *IEEE CICC*, pp. 1-4, 2015. I thank all the co-authors for their valuable advice in designing and testing of the prototypes.

followed. Finally, the measurement results are shown, followed by the conclusion.

### 3.1.1 Introduction

Conventional $\Delta\Sigma$ ADCs rely on the use of operational transconductance amplifiers (OTAs). However, they are scaling unfriendly, and consume large chip area and power. They also require high gain (e.g., 60 dB) to ensure linearity and accuracy; however, such high gain is hard to achieve in advanced CMOS process with reduced transistor intrinsic gain. In addition, the reduced supply voltage makes it hard to stack transistor vertically for gain boosting. A small supply voltage also leads to reduced signal swing and dynamic range. The advent of nanometer technology calls for a new design methodology for $\Delta\Sigma$ ADC that not only does not suffer from CMOS scaling but actually benefits from it.

An emerging and promising approach to design $\Delta\Sigma$ ADCs is to use voltage controlled oscillators (VCOs) built with a ring of inverters [Taylor and Galton [2013]; Reddy et al. [2012]; Straayer and Perrot [2008]; Lee et al. [2013a]; Park and Perrot [2009]; Rao et al. [2014]; Young et al. [2014]]. Ring VCOs act as both integrators and quantizers in the phase domain. Thus, they can replace OTA-based integrators and flash quantizers in conventional $\Sigma\Delta$ ADCs. VCO-based ADC are simple, low-power, small area, and operate well under low voltage supply. Moreover, their performance naturally improves with CMOS scaling. The increased transistor speed ($f_T$) and reduced inverter delay lead to higher VCO tuning gain and timing resolution. The reduced transistor capacitance leads to lower VCO power.

Despite the many merits mentioned above, VCO-based ADCs have one ma-

jor limitation, which is VCO's nonlinear frequency tuning characteristic. Several techniques have been proposed to address this issue. Digital calibration can be used for open-loop VCO-based ADCs [Taylor and Galton [2013]; Rao et al. [2014]]. This method is mostly digital, but it depends on the accurate matching between the main signal path and the replica path, which is hard to guarantee in the presence of PVT variations. Another method is to embed the VCO in a feedback loop with an analog filter preceding it [Straayer and Perrot [2008]]. This way, the VCO nonlinearity is suppressed by the filter gain. However, this method still requires conventional OTAs to build the filter, which is undesirable. In addition, this method uses VCO only as a quantizer, and thus, the VCO input signal swing is still large, causing large distortions. To reduce the VCO input swing, one approach is to perform residue cancelation [Reddy et al. [2012]]. The other approach is to use VCO as an integrator by outputting phase instead of frequency [Lee et al. [2013a]; Park and Perrot [2009]; Young et al. [2014]]. To further reduce nonlinearity, dual VCO based integrator can be used to suppress VCO's dominant second-order distortion [Lee et al. [2013a]].

This section presents a low-power and small-area closed-loop OTA-free $\Delta\Sigma$ ADC. It uses ring VCO to perform both integration and quantization. There are two key novelties for this work. First, the proposed ADC is mostly digital and highly modular. It is comprised of an array of *identical* circuit slices. Each slice performs a local integration, a 1-bit quantization, and a 1-bit current feedback. To our best knowledge, our work is the first fully distributed $\Delta\Sigma$ ADC. Its topology is exactly opposite to the conventional architecture whose integration, quantization, and feed-

back functions are lumped at separated circuit blocks. The repetitive and distributed architecture of the proposed ADC greatly reduces the design complexity, and allows it to be easily configured for different resolution specifications. To construct a $m$-bit $\Delta\Sigma$ ADC, we can simply arrange $(2^m - 1)$ slices in a ring. The slice layout is designed to be a rectangle with I/O on the two sides. Thus, when two slices are placed nearby, they naturally connect to each other. Such arrangement significantly reduces the layout effort.

One challenge for having a distributed architecture and layout is that the DAC elements are no longer grouped together, but spread out over the entire ADC area. The longer distance and less well matched surrounding environment causes larger mismatches. Moreover, in order to embed a DAC inside a small slice layout to reduce chip area and minimize wiring capacitance, the DAC area needs to be small, which further increases mismatch. The second key novelty of this work is that it proposes a novel DAC calibration technique that both digitally senses and removes DAC mismatch errors. It has low hardware complexity by taking advantage of the intrinsic clocked level averaging (CLA) capability of dual-VCO-based integrator [Lee et al. [2013a]]. It ensures high linearity regardless of the VCO center frequency.

A prototype ADC designed in 130nm occupies an area of only 0.04mm$^2$. It achieves 71dB SNDR over 1.7MHz BW while sampling at 250MS/s and consuming only 0.9mW from a 1.2V power supply. The corresponding figure-of-merit (FOM) is 98 fJ/conversion-step, which compares favorably to the state-of-the-art VCO-based $\Delta\Sigma$ ADCs.

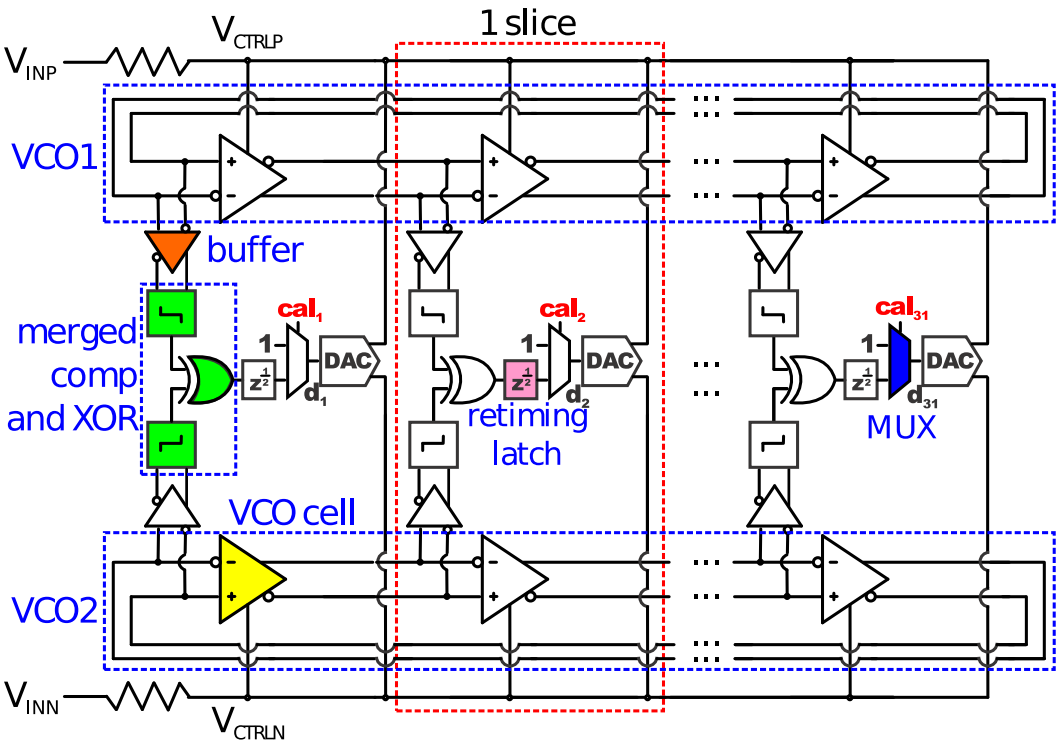


Figure 3.1: Architecture of the proposed VCO-based ΣΔ ADC.

### 3.1.2 Proposed ADC Architecture

Fig. 3.1 shows the proposed closed-loop ΔΣ ADC. The input resistor converts the ADC input voltage to current. The subtraction between the input current and the DAC feedback current happens at the VCO control nodes. The residue current goes into the VCO and is integrated in the phase domain. To reduce power consumption, no extra current is supplied for the VCO. In other words, the VCO is solely powered up by the residue current. The ADC core consists of 31 identical slices. The VCO cell is a cross-coupled differential inverter [Fig. 3.2(a)]. The buffer [Fig. 3.2(b)] isolates the VCO from the kickback noise from the comparator.

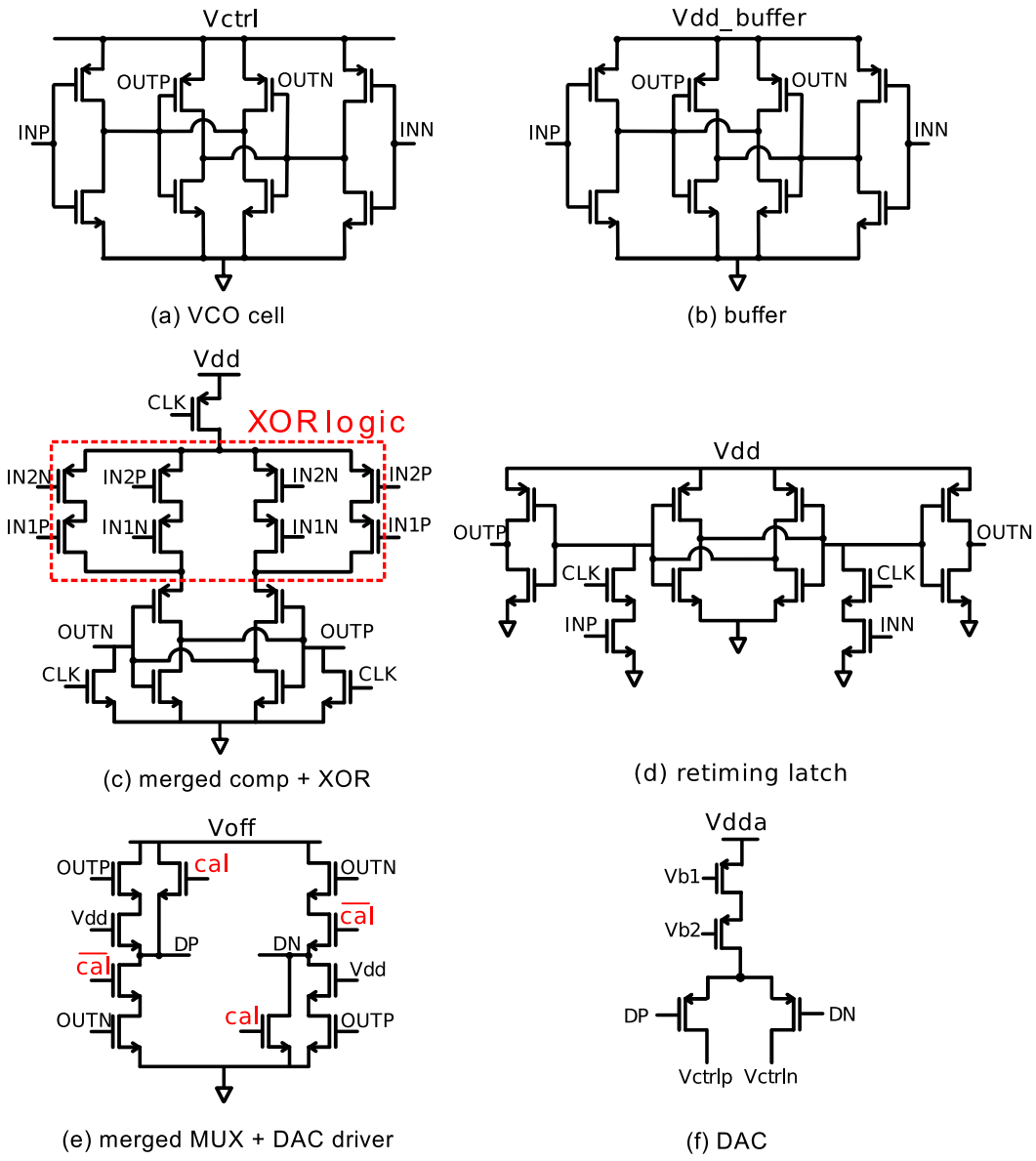


Figure 3.2: Individual block schematic.

It has the same structure as a VCO cell but with a smaller size. Due to the low swing of the output of a VCO cell, a separate power supply (0.5V) is assigned to the buffer.

The comparator samples the VCO phase every clock period and the XOR gate performs phase comparison. Note that although the two comparators and the XOR are separately drawn in Fig. 3.1, they are merged into a single strong-arm latch with an embedded XOR logic [Fig. 3.2(c)]. It saves power, reduces area, and shortens the overall delay. The retiming latch [Fig. 3.2(d)] with half clock cycle delay is added to remove input-dependent comparator delay. It embeds the make-before-break scheme so as to minimize the glitch during DAC switching, which otherwise produces distortion. The low swing DAC driver [Fig. 3.2(e)] is used to reduce the coupling from the DAC control terminals to the output [Park and Perrot [2009]]. The cascode PMOS DAC is in Fig. 3.2(f). Thanks to the proposed digital DAC calibration scheme which will be explained later, the DAC matching requirement is significantly relaxed and a small DAC can be used.

The VCO nonlinearity issue is solved in the proposed ADC for the following reasons: 1) the VCO acts as an integrator that provides gain, and thus, the signal component at the VCO input is small; 2) the total DAC element is 31 (5-bit), and thus, the quantization noise component at the VCO input is also small; 3) the differential VCO structure cancels out the major VCO second-order distortion. Measurement results confirm that the VCO-induced distortion is below $-75$ dBFS.

The distributed and modular structure of the proposed ADC greatly simplifies the layout. As shown in Fig. 3.3(a), each repetitive slice is laid out as a rectangular box. The entire ADC can be formed by simply aligning 31 slices on a track [see Fig. 3.3(b) where numbers and arrows indicate direction]. This brings several merits. First, the layout is very compact. The connected circuit blocks within each

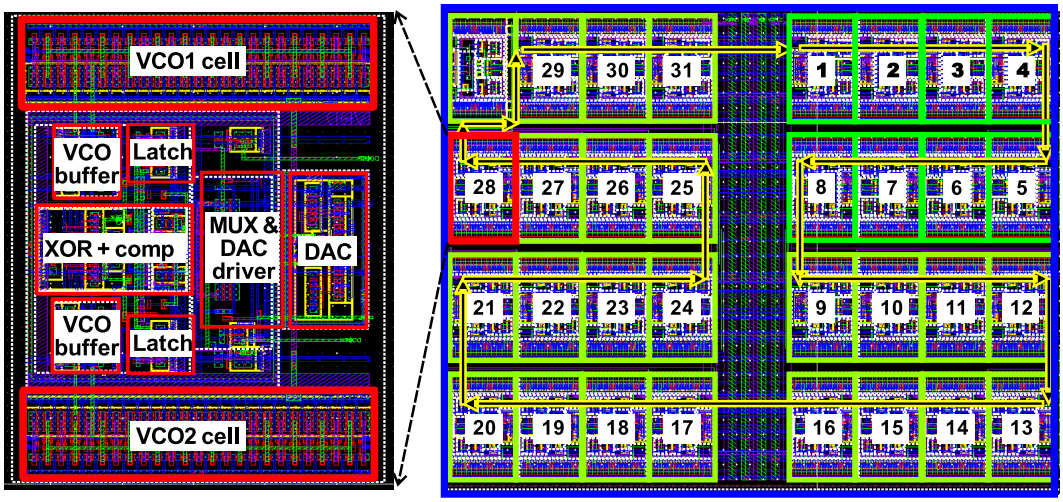


Figure 3.3: Layout of each slice and the ADC core.

slice are placed very close to each other with shortest wires and minimum parasitics. It reduces chip area, shortens delay, and saves power. Second, the layout is simple, digital like, and configurable. The input and output ports are located on the same horizontal lines at the two sides of a slice. Thus, two slices can be automatically connected when placed next to each other. The proposed layout design allows quick change to the number of slices for different resolution specifications.

Global signals, such as clock, Vdd, Gnd, and VCO control nodes ($V_{ctrl_N}$ and $V_{ctrl_P}$) are placed at the center of the ADC [Fig. 3.3(b)]. This provides matching for the two sides. It also facilitates clock and power distribution by minimizing horizontal distances. To improve matching accuracy, dummy slices are added at the peripheral of the ADC core. Note that the empty space at the ADC center causes slight VCO load mismatches between the slices at the center and those away from

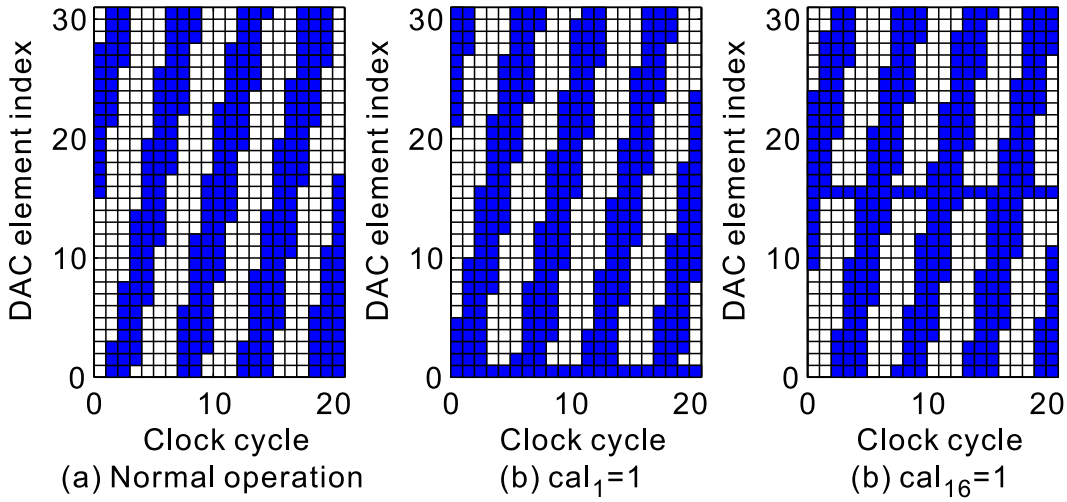


Figure 3.4: Measured DAC element selection pattern.

the center, which results in a small phase non-uniformity. However, because the phase error is high-pass shaped by the loop, its overall effect is negligible. Finally, to reduce coupling, power domains are separated for sensitive circuits (VCO and DAC) and non-critical blocks (comparator, XOR, and latch). Guard ring is also added to provide further isolation.

### 3.1.3 Novel Digital DAC Calibration

Since small-area distributed DAC elements are used, they have large mismatches, which can severely degrade the ADC linearity. To address this issue, a novel digital calibration technique with low hardware complexity is proposed. It only adds a MUX before the DAC [Fig. 2.10]. The MUX can be merged with a low-swing DAC driver [Fig. 3.2(f)]. When $cal = 0$, the driver output follows its input. When $cal = 1$, the driver output is forced to 1.

During normal operation ($cal_i = 0$), the DAC selection follows the intrinsic clocked averaging (CLA) behavior Lee et al. [2013a]. It is shown in Fig. 3.4(a) where a solid box means its corresponding DAC element is on. The selection pattern shifts every clock cycle at the rate of twice the VCO center frequency.

During calibration mode, both ADC inputs are shorted to $V_{cm}$. First, $cal_1$ is set to 1. Thus, the first DAC element is always on regardless of the XOR output [Fig. 3.4(b)]. Since the VCO is an ideal integrator with infinite gain in the phase domain, the long-term average of the DAC output must equal to $31/2 = 15.5$. Thus, we have:

$$[1, p_{1,2}, ..., p_{1,31}] \times [1 + e_1, 1 + e_2, ..., 1 + e_{31}]^T = 15.5 \tag{3.1}$$

where $\{e_i\}$ represents DAC mismatch; $\{p_{1,i}\}$ denotes the probability of $i$-th DAC element being on and can be measured by averaging the DAC input $\{d_i\}$ over a large number (e.g., $10^3$) of samples. After $\{p_{1,i}\}$ are extracted, $cal_1$ is reset to 0 and $cal_2$ is set to 1. We measure $\{p_{2,i}\}$ and have:

$$[p_{2,1}, 1, ..., p_{2,31}] \times [1 + e_1, 1 + e_2, ..., 1 + e_{31}]^T = 15.5 \tag{3.2}$$

The same process is repeated for all other DAC elements [see Fig. 3.4(c) for the DAC selection pattern at $i = 16$]. Thus, a matrix of 31 equations can be formed:

$$\begin{pmatrix} 1 & p_{1,2} & \cdots & p_{1,31} \\ p_{2,1} & 1 & \cdots & p_{2,31} \\ \vdots & \vdots & \ddots & \vdots \\ p_{31,1} & p_{31,2} & \cdots & 1 \end{pmatrix} \begin{pmatrix} 1 + e_1 \\ 1 + e_2 \\ \vdots \\ 1 + e_{31} \end{pmatrix} = \begin{pmatrix} 15.5 \\ 15.5 \\ \vdots \\ 15.5 \end{pmatrix} \tag{3.3}$$

Thus, we can solve $\{e_i\}$ by inverting (3.2). Once $\{e_i\}$ are obtained, DAC mismatch errors can be easily removed from ADC output as in [Kauffman et al. [2014]]. The

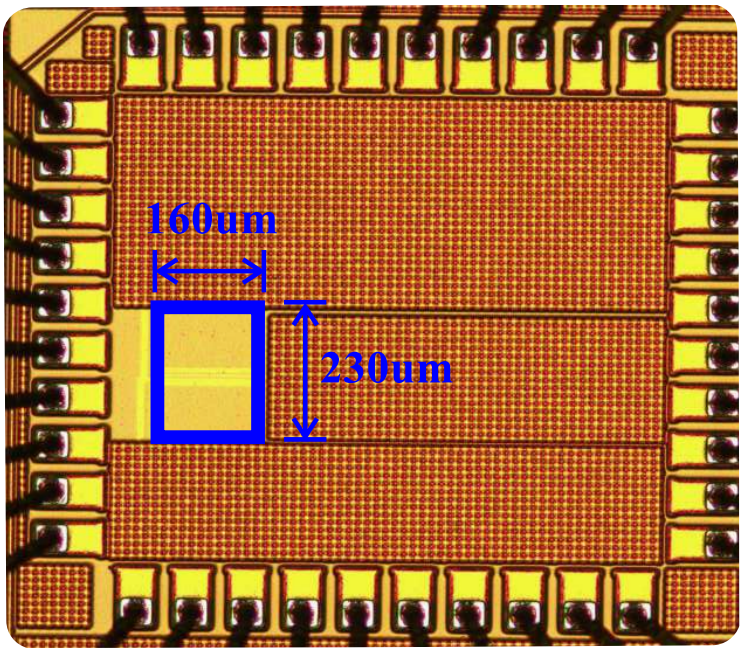


Figure 3.5: ADC die photo

solving of $\{e_i\}$ is done off-chip in this design, but since it is purely digital, it can be easily synthesized and integrated on chip. In addition, because we only need to solve $\{e_i\}$ once per calibration, the required power is negligible.

### 3.1.4 Measurement Results

The prototype ADC occupies 0.04mm$^2$ in 130nm CMOS [Fig. 3.5]. It samples at 250MS/s and has a bandwidth of 1.7MHz at the OSR of 75. It consumes 0.9mW from a 1.2V supply.

The extracted DAC mismatch errors $\{e_i\}$ in percentage using the proposed calibration technique is shown in Fig. 3.6. Because the DAC element is small ($12\mu m$ by $7\mu m$) and distributed, their mismatches can be as large as 8%. The

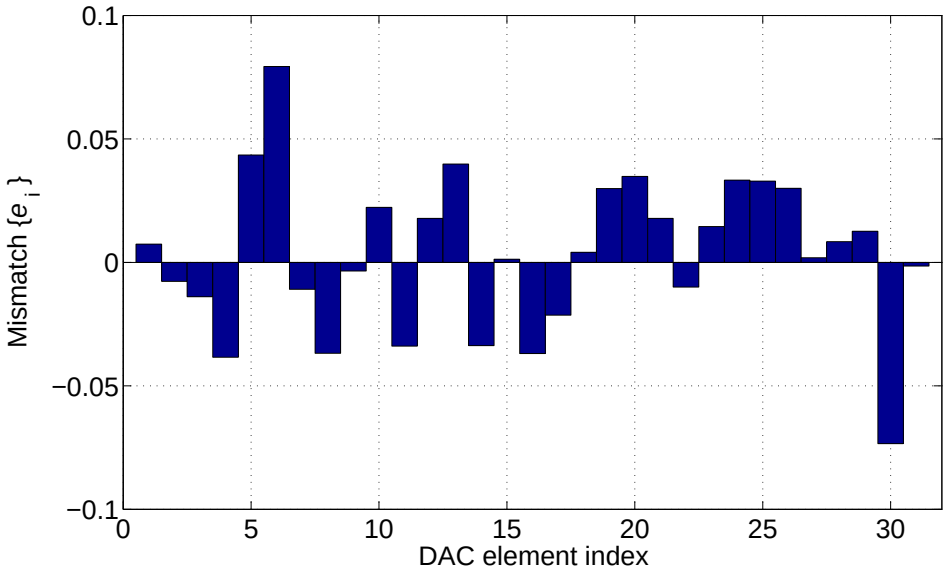


Figure 3.6: Extracted DAC mismatch errors

standard deviation is 3.1%.

Fig. 3.7 shows the measured ADC spectrum at $f_{in} = 500$kHz. The measured SNDR before calibration is 67.1dB. This performance is made possible by the intrinsic CLA-based DEM that upshifts the majority of the DAC mismatch errors to twice the VCO center frequency at 29.1MHz [Lee et al. [2013a]]. However, CLA cannot completely remove the in-band mismatch error, which results in an increased noise floor. After digital DAC calibration, the in-band mismatch noise is removed, leading to an improved SNDR of 70.6dB. Measurement shows that $2^{10}$ points are sufficient for an accurate extraction of $\{e_i\}$. Fig. 3.8 shows measured SNDR versus input amplitude before and after calibration. The post-calibration dynamic range is 74dB.

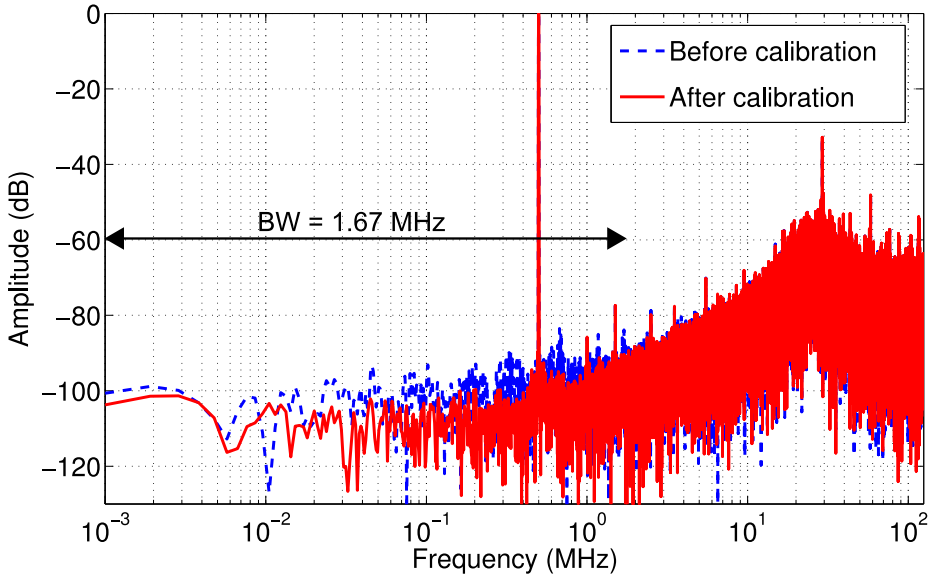


Figure 3.7: Measured ADC spectrum before and after calibration ($2^{18}$ points).

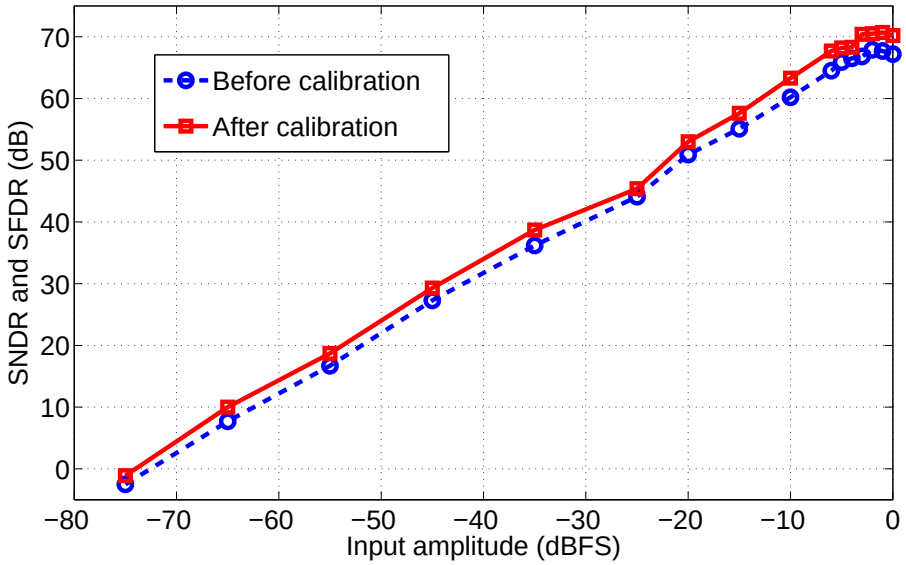


Figure 3.8: Measured SNDR and SFDR vs. input amplitude at $f_{VCO}$ = 29.4MHz

The overall ADC performance is summarized in Table 1. Its Walden figure-of-merit (FOM) is 98 fJ/conv-step, which compares favorably to the state-of-the-art VCO-based $\Delta\Sigma$ ADCs, especially considering its relatively old 130nm process. Because the proposed ADC is scaling friendly, its performance naturally improves with CMOS scaling. Our simulation study shows that the same ADC design can achieve an FOM of 20 fJ/conv-step if implemented in 65nm process.

Table 3.1: Comparison with other continuous-time $\Delta\Sigma$ ADCs

| | **This work** | Taylor [2013] | Rao [2014] | Straayer [2008] | Reddy [2012] | Park [2009] | Young [2014] |
|---|---|---|---|---|---|---|---|
| Process [nm] | **130** | 65 | 90 | 130 | 90 | 130 | 65 |
| fs [MHz] | **250** | 2400 | 640 | 950 | 600 | 900 | 1280 |
| BW [MHz] | **1.67** | 37.5 | 5 | 10 | 10 | 20 | 50 |
| SNDR [dB] | **70.6** | 70 | 73.9 | 72 | 78 | 78 | 64 |
| Power [mW] | **0.91** | 39 | 4.1 | 40 | 16 | 87 | 38 |
| Area [$mm^2$] | **0.04** | 0.08 | 0.16 | 0.41 | 0.36 | 0.45 | 0.49 |
| FOM [fJ/conv] | **98** | 201 | 101 | 615 | 125 | 330 | 294 |

## 3.2 Purely-VCO-Based Second-Order $\Delta\Sigma$ ADC

The second section[2] of this chapter reports a VCO-based single-loop continuous-time (CT) $\Delta\Sigma$ analog-to- digital converter (ADC) that does not need any OTA-based analog integrator. It achieves the second-order noise shaping by cascading two VCO-based integrators and removing the sampling operation in the first VCO-based integrator. Behavioral simulations confirm the validity of the proposed ADC

architecture.

This section is organized as follows: an introduction is first presented. The proposed purely-VCO-based high-order $\Delta\Sigma$ ADC achritecture is discussed next. Simulation results are shown, followed by the conclusion.

### 3.2.1 Introduction

CT $\Sigma\Delta$ ADCs have an advantage over discrete-time (DT) ones for low-power applications. No settling behavior is involved, which otherwise requires power-consuming operational transconductance amplifiers (OTAs) with high unity-gain bandwidths in switched-capacitor circuits. It makes higher-frequency operation possible. CT ADCs also possess inherent anti-aliasing capability. In addition, the input sampling is done after the loop filter. Thus, any sampling error is suppressed by the loop filter along with the quantization noise [Yan and Sanches-Sinencio [2004]]. One drawback for conventional CT $\Delta\Sigma$ ADCs is that they rely on the use of OTA-based analog integrators that are power hungry and scaling unfriendly.

Recently, there have been emerging efforts to use ring VCOs to build CT $\Sigma\Delta$ ADCs. VCOs can act as both integrators and quantizers in the phase domain, and thus, can replace OTA-based analog integrators and voltage comparators used in conventional $\Sigma\Delta$ ADCs. The advantage for VCOs is that they are scaling friendly, and thus, consume low area and power in advanced nanometer CMOS

[2]This section is a reprint of the publication: Yeonam Yoon, Kyoungtae Lee, and Nan Sun, "A purely-VCO-based single-loop high-order continuous-time delta sigma ADC", *IEEE ISCAS*, pp. 926-929, 2014. I thank all the co-authors for their valuable advice in designing and testing of the prototypes.

processes. Moreover, the VCO resolution, set by the inverter delay, naturally improves with CMOS scaling. So far, many first-order VCO-based $\Delta\Sigma$ ADCs have been developed [Lee et al. [2013a]; Taylor and Galton [2010]; Lee et al. [2013b]]. Despite their design simplicity, they achieve only first-order shaping and require a large over-sampling ratio (OSR) to guarantee a reasonable SNDR, leading to a large sampling rate and clock power. Researchers have attempted to achieve higher-order noise shaping by using the multi-stage noise shaping (MASH) structure [Hernandez [2012]; Yu et al. [2013]]; however, the loop mismatches cause noise leakage and limit the ADC performance. Another method to achieve high-order shaping is to place conventional OTA-based analog integrators in front of the VCO [Straayer and Perrot [2008]; Park and Perrot [2009]]. Nevertheless, since the first several integrator stages that dominate ADC power and noise still use OTAs, the overall ADC performance enhancement brought by using a VCO-based last stage is limited.

This section presents a single-loop second-order VCO-based CT $\Sigma\Delta$ ADC. It is constructed by cascading two novel VCO-based integrators [Lee et al. [2013a,b]]. Note that the phase for any ring VCO is intrinsically quantized; in other words, any VCO has an inherent built-in quantizer. Thus, we have to figure out a way to deal with the quantization noise from the first VCO-based integrator, as its quantization noise can only be first-order shaped. The proposed VCO-based integrator addresses this problem by naturally performing a pulse width modulation (PWM) of its input, and thus, the quantization error is moved out of the signal band. Moreover, unlike the conventional VCO-based integrator that uses a reference sampling clock

[Park and Perrot [2009]], the proposed VCO-based integrator operates in a truly CT fashion, which prevents the high-frequency quantization noise to be aliased back into the signal band. As a result, the intrinsic quantization noise problem in the first-stage integrator is solved, leading to the true second-order noise shaping in a single-loop VCO-based $\Delta\Sigma$ ADC. Compared to prior arts, it does not suffer from loop mismatches [Hernandez [2012]; Yu et al. [2013]] and completely obviates the need for conventional analog integrators [Straayer and Perrot [2008]; Park and Perrot [2009]], thereby reducing power and area.

### 3.2.2 Second-Order Noise Shaping Using VCOs

Researchers have long desired a purely-VCO-based high-order CT $\Delta\Sigma$ ADC architecture that obviates the need for analog integrators. However, it has not been developed due to a number of difficulties. First, in order to use a VCO as an integrator, its phase must be taken out as the output variable, instead of the frequency (phase is proportional to integration of the VCO input, while frequency is not). Most existing VCO-based ADCs can only output the digitized frequency [Straayer and Perrot [2008]; Taylor and Galton [2010]]. They sample the outputs of all VCO delay cells and compare them with the values sampled at the previous clock cycle, so that the phase change, which is essentially the frequency, is extracted. However, if frequency is the output, the nice integration property of the VCO is lost. Recently, researchers have developed a technique that can measure the VCO phase [Park and Perrot [2009]]. It also samples the VCO delay cells, but instead of comparing them with their previously sampled values, it compares them

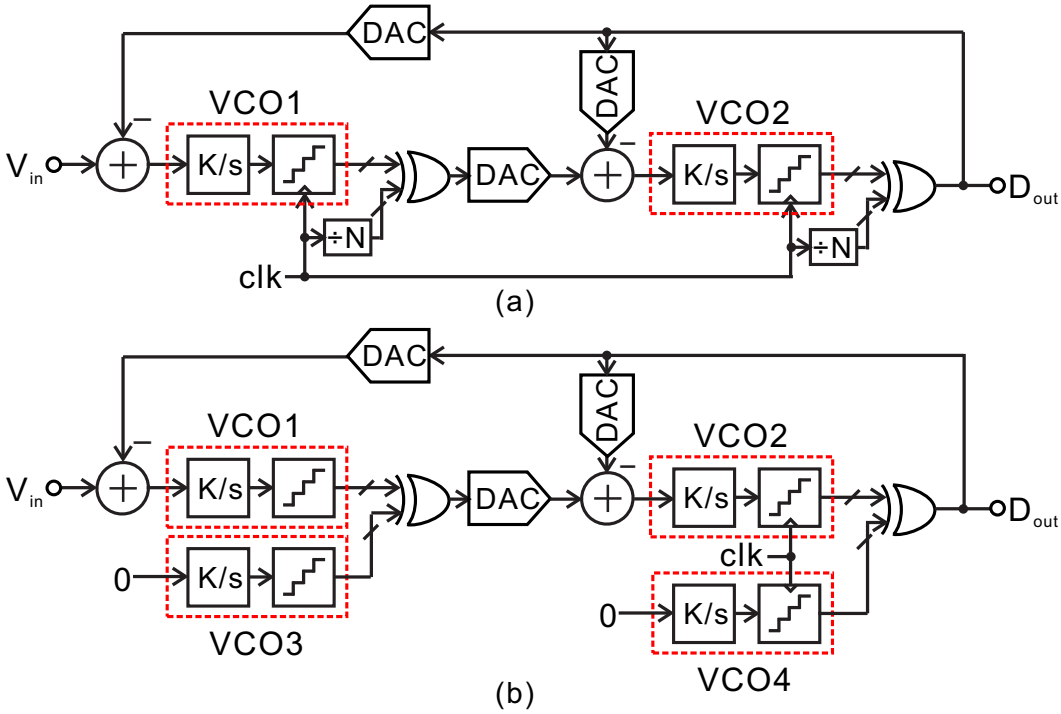


Figure 3.9: (a) Existing VCO-based integrators. (b) Proposed implementation.

with a set of reference phases derived from the sampling clock [Park and Perrot [2009]].

Based on this scheme, a natural extension to build a second-order CT $\Delta\Sigma$ ADC would be to cascade two of these VCO-based integrators and wrap a feedback loop around them, as shown in Fig. 3.9(a). Nonetheless, this scheme does not work for two reasons. First, because the output of the first VCO-based integrator (VCO1) is sampled, the ADC does not operate in a truly CT manner. Second, a VCO cannot produce an output phase with continuous amplitude; its phase is inherently quantized. For example, an $N$-stage ring VCO can only produce $2N$ discrete phases, which is different from a standard analog integrator whose output

voltage is continuous in amplitude. As a result, any VCO produces intrinsic quantization noise, and this noise is aliased into the signal band if sampled. Note that the aliased quantization noise from VCO1 is only first-order shaped. Thus, even though the quantization noise from VCO2 is shaped to the second order, the overall noise shaping is only first order, as the in-band noise is dominated by that from VCO1.

To address these issues and achieve the second-order shaping, a novel VCO-based $\Delta\Sigma$ ADC is proposed [see Fig. 3.9(b)]. In this architecture, the phase of VCO1 is taken out by comparing its output stages with those from VCO3, which is simply a copy of VCO1 but with a zero input. In real circuit implementation, VCO3 is connected to the negative input $V_{inb}$, thus forming a differential setup. Since the proposed comparison scheme operates in a CT way without sampling, a true CT behavior is ensured. Furthermore, because no sampling is involved, there is no aliasing of high frequency quantization noise from VCO1 and VCO3. However, it does not remove any quantization noise, which can still dominate the overall in-band quantization noise. Simulations show that if standard quantizers are used in the model of Fig. 3.9(b), the overall noise shaping is only first order even though the quantizer operates in a CT manner.

The most important feature to note is that the way a VCO phase quantizer works is drastically different from that of a standard quantizer. This difference brings a fundamental advantage to the VCO phase quantizer, which solves its quantization noise problem. Fig. 3.10(a) shows the behavior of a standard voltage quantizer with a ramp input. The output follows a staircase waveform; it does not change unless the input crosses a quantizer threshold. Fig. 3.10(b) shows the input/output

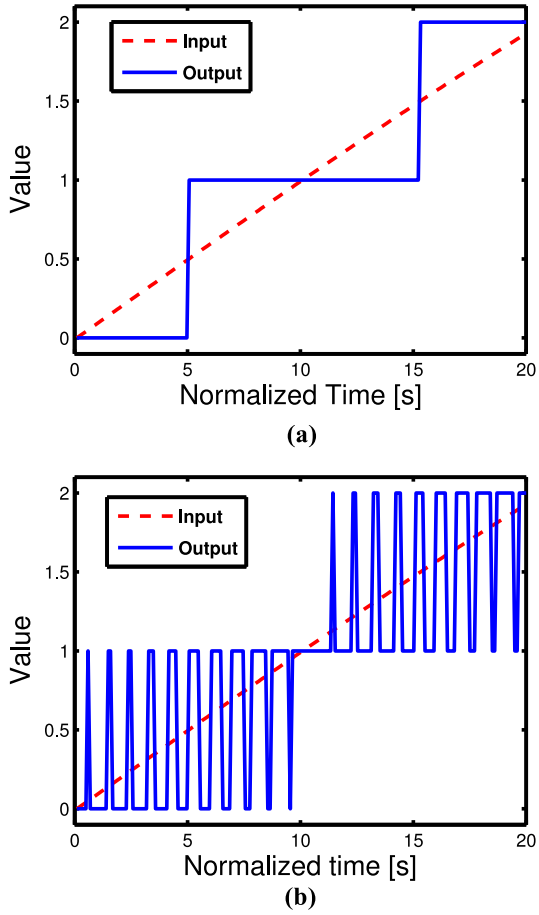


Figure 3.10: Behaviors of (a) a standard quantizer and (b) a VCO phase quantizer.

characteristics for a VCO intrinsic phase quantizer. There is no clear threshold. The output is constantly varying because the VCO phase keeps advancing with an average rate of its center frequency. The result is that the VCO phase quantizer essentially performs PWM of its input [Rao et al. [2011]]. This intrinsic phase quantization property is exploited in the proposed VCO-based integrator.

The proposed VCO-based integrator is shown in Fig. 3.11(a). It consists of

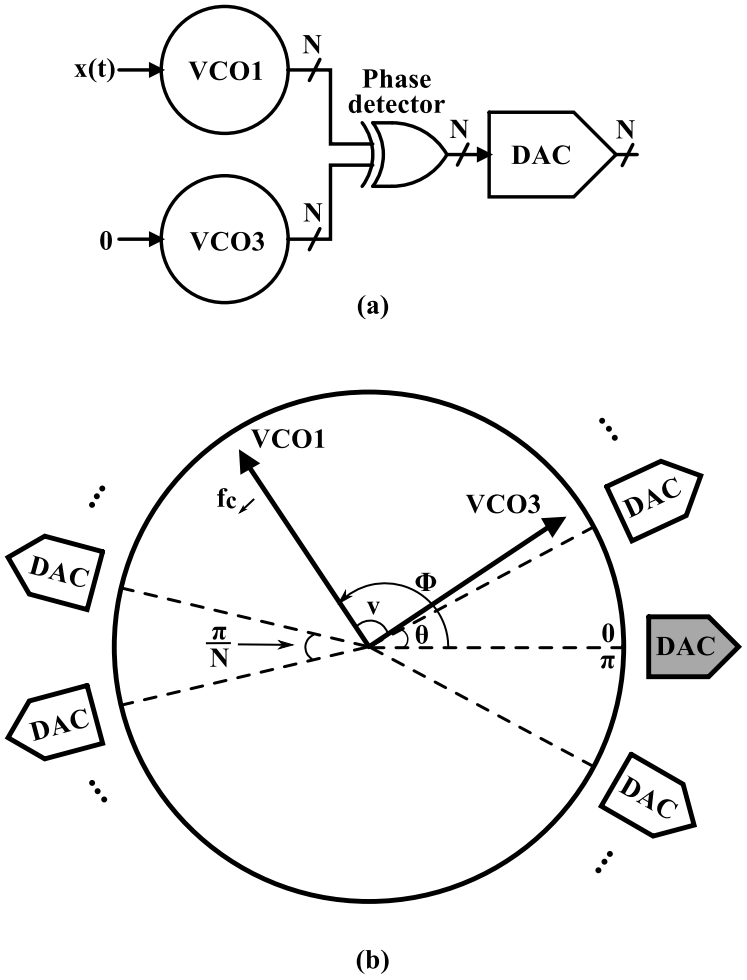


Figure 3.11: (a) Proposed VCO-based integrator, and (b) its operation principle.

two identical VCOs, an array of $N$ XOR gates and $N$ 1-bit DACs. Here, the input to VCO3 is connected to zero, but it can be connected to $-x(t)$ in a differential structure. Fig. 3.11(b) shows its operation principle. Here, $\theta$ is the phase of VCO3 which serves as a reference for VCO1, and $v$ is the phase difference between VCO3 and VCO1. Note that since one entire VCO period means going around the ring VCO twice, the corresponding phase range for the VCO loop shown in Fig. 3.11(b)

is from 0 to $\pi$, not $2\pi$. The phase of VCO1 can be represented as

$$\begin{aligned}\Phi(t) &= \int_0^t 2\pi[K_{VCO}x(t) + f_c]\mathrm{dt} \\ &= 2\pi K_{VCO}\int_0^t x(t)\mathrm{dt} + 2\pi f_c t \equiv v + \theta \end{aligned} \tag{3.4}$$

where $K_{VCO}$ is the VCO tuning gain and and $f_c$ is its free running frequency (center frequency). $\theta$ increases at the speed of $f_c$, and $v$ varies according to the input. Since the VCO has $N$ stages, its phase quantization step is $\pi/N$. The phase difference is detected using $N$ XOR gates, which drive the 1-bit DAC array. As shown in Fig. 3.10, each DAC can be mapped to a phase on the VCO ring. Out of the $N$ DACs, the ones that are turned on (with corresponding XOR outputs being 1) are in the arc of $v$.

Since all DACs operate in a similar way, it is sufficient to study the behavior of only one DAC. For simplicity, let us examine the operation of the DAC at phase 0 (the shaded DAC in Fig. 3.11(b)). As explained earlier, it is selected only when the arc of $v$ contains it. Mathematically speaking, it means that the DAC input is 1 when:

$$\theta + v > \pi \quad \rightarrow \quad v > \pi - \theta \tag{3.5}$$

Here $\theta$ is wrapped into $[0, \pi]$. In other words, whenever it goes beyond $\pi$, we subtract it by $\pi$.

Fig. 3.12(a) shows the equivalent operation of the VCO-based integrator following the relationship of (3.5). Since $\theta$ increases from 0 to $\pi$, $(\pi - \theta)$ is drawn

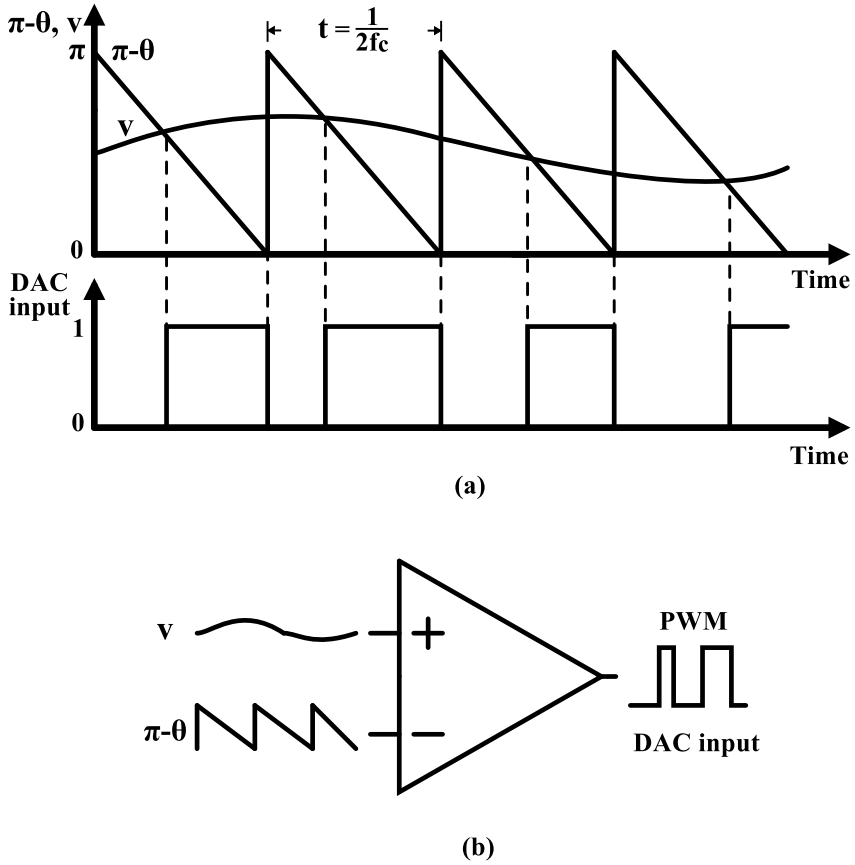


Figure 3.12: (a) PWM behavior of VCO-based integrator, (b) equivalent circuit.

from $\pi$ to 0. Dashed lines indicate the regions which satisfy the condition of (3.5). As clearly seen, PWM signals are generated at the XOR output. This operation is the same as that of the natural-sampling leading-edge PWM. It is well-known that the ideal PWM operation does not produce distortions in the signal band, and the tones are located around the PWM carrier frequency and its harmonics [Rao et al. [2011]]. Here in our case, the PWM carrier frequency is $2 \times f_c$, not $f_c$, because 1 VCO period means going around the VCO ring twice (see Fig. 3.12).

Due to the aforementioned reasons, the amplitude information of the input is not lost in the proposed VCO-based integrator, but is faithfully captured in the output pulse width. Therefore, the VCO-based integrator produces a much more accurate representation of the input than a standard quantizer. The effective in-band (low frequency) quantizer resolution is much higher, and thus, the quantization noise issue in the first VCO-based integrator is solved. From a frequency domain perspective, although the total quantization noise power of the VCO phase integrator is identical to that of a standard quantizer for the same quantization step, their frequency domain distributions are significantly different. For the VCO-based integrator, due to its PWM behavior, its quantization noise in the signal band is very small, and most of the noise is concentrated around the PWM carrier frequency at $2f_c$. This high-frequency noise is sufficiently suppressed by the second-stage integrator that works as a low-pass filter. As a result, the total amount of quantization noise from the first stage VCO that shows up at the ADC output is negligible. Consequently, almost ideal second-order noise shaping can be achieved with the proposed architecture of Fig. 3.9(b), even though the first VCO-based integrator produces quantization noise.

Fig. 3.13 shows 4,096 point FFT plots for a standard quantizer and a VCO-based integrator. As clearly can be seen in Fig. 3.13(a), low-frequency quantization noise of the VCO-based integrator is lower than that of the standard quantizer. In Fig. 3.13(b), we can see concentrated noise around harmonics of PWM carrier frequency. This quantization noise is shaped due to the feedback operation.

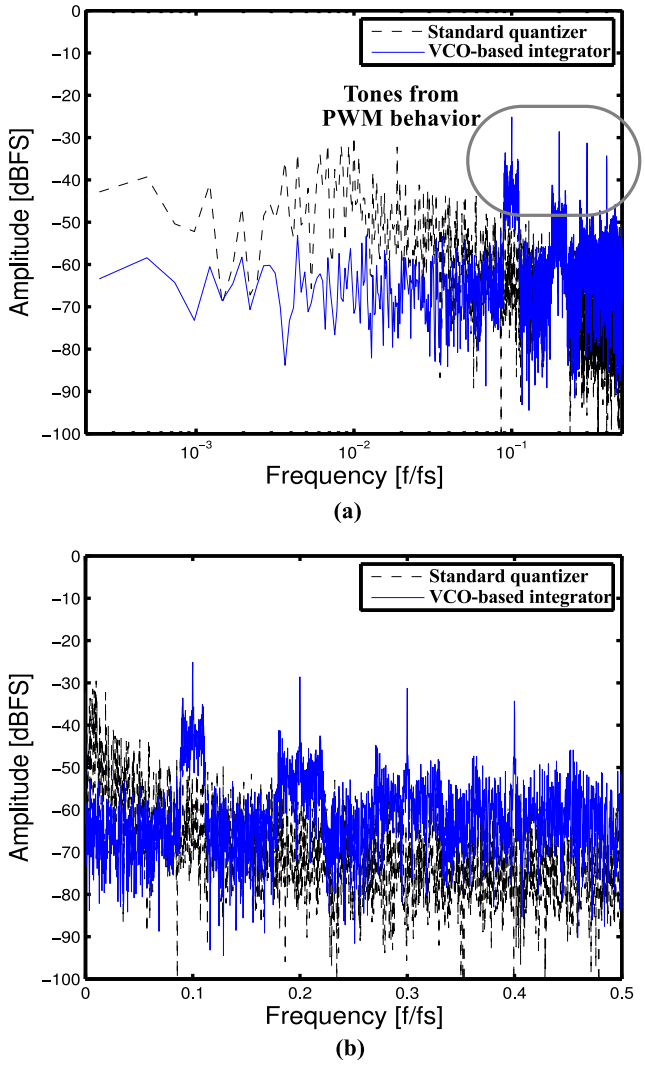


Figure 3.13: Quantization noise spectrum in (a) logarithmic and (b) linear scale.

### 3.2.3 Behavioral Simulations

To verify the proposed ADC architecture, behavioral-level simulations have been performed in SIMULINK that conveniently provides built-in CT VCO models. The VCOs used in the ADC contain 15 delay cells each. The gains for VCOs

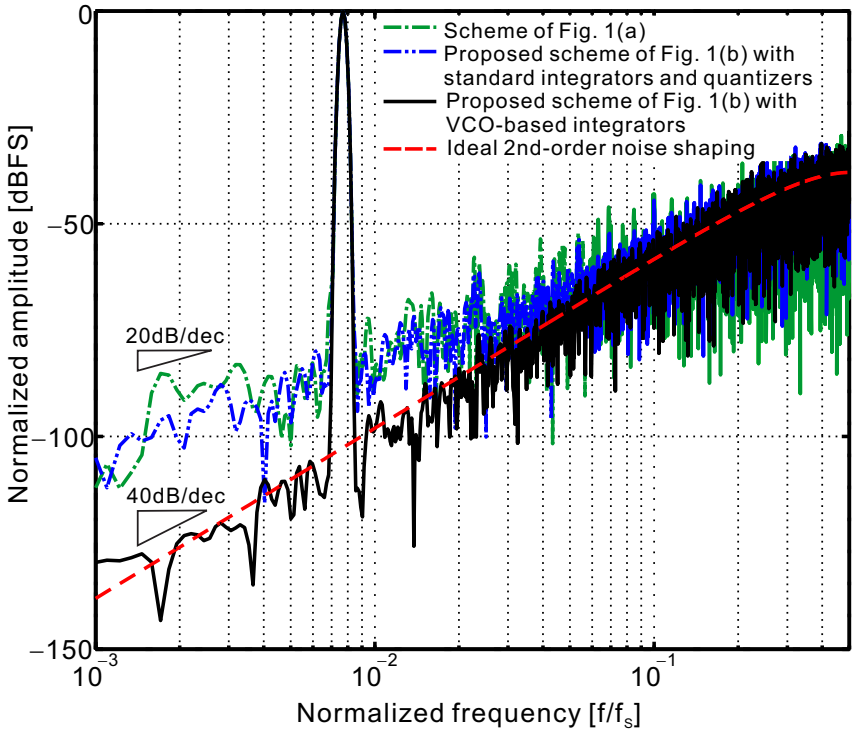


Figure 3.14: Simulated ADC output spectra.

and DACs are chosen in such a way that the noise transfer function for the second-stage VCO quantization noise gives ideal second-order shaping $(1 - z^{-1})^2$. Fig. 3.14 shows the simulation results for various configurations. As can be seen, the $\Delta\Sigma$ ADC that uses existing VCO-based integrators of Fig. 3.9(a) produces only first-order noise shaping. The SQNR at the OSR of 30 is only 59 dB. The reason is that the sampling operation in VCO1 aliases its quantization noise into the signal band, which can only be shaped to the first order. Fig. 3.14 also shows that even if the proposed ADC architecture of Fig. 3.9(b) is used but with standard quantizers, the overall noise shaping remains only first order, because the quantization noise from the first stage still dominates the in-band noise. Its SQNR of 64 dB is higher

than the prior case due to the removal of aliasing, but the improvement is limited. By contrast, if the proposed architecture adopts the novel VCO-based integrators, almost ideal second-order noise shaping obtained. The SQNR is substantially improved to 81 dB. The intrinsic quantization noise problem of the first VCO-based integrator is solved because the PWM behavior of the VCO phase quantizer ensures very low in-band quantization noise and moves the majority of the noise to very high frequencies. These simulation results match well with the theoretical analyses and firmly prove the feasibility of the proposed VCO-based high-order CT $\Delta\Sigma$ ADC architecture.

## 3.3 Conclusion

The first section presented a scaling friendly VCO-based $\Delta\Sigma$ ADC with small area and low power. It has an interesting distributed and modular architecture, which reduces design efforts and allows easy layout generation and reconfiguration for different resolution requirements. Because the proposed ADC is highly digital and regular, it also opens the door for both schematic and layout design automation. This work also proposed a novel digital DAC mismatch calibration technique, which ensures a high linearity even in the presence of 8% DAC mismatch. It allows the significant reduction of DAC area. This is critical for further ADC chip area shrinking in advanced CMOS processes, as other ADC components are completely digital, such as inverter, latch, and XOR.

The second section presented a purely-VCO-based single-loop second-order CT $\Delta\Sigma$ ADC. It can be easily generalized to achieve even higher order noise shap-

ing. In the proposed VCO-based integrator, its intrinsic quantization noise is moved out of band due to its inherent PWM property. A true CT operation also makes sure that the high-frequency quantization noise is not aliased back to the signal band. The proposed VCO-based $\Delta\Sigma$ ADC does not require any area/power consuming OTA-based analog integrator used in conventional $\Delta\Sigma$ ADCs. Because of its scaling compatibility, it is envisioned that it can achieve superior performance in advanced CMOS technologies.

# Chapter 4

# Twp-Step SAR/SS ADC

This chapter presents a column-parallel SAR/single-slope ADC exploiting $kT/C$ noise cancellation using analog correlated double sampling (CDS) for a CMOS image sensor (CIS). Inputs are quantized by SAR and SS sequentially in a two-step way. To reduce the capacitor area of SAR, which is one of the main disadvantage, single-slope ADC is added with minimal hardware change. Analog CDS is embraced to cancel the comparator offset. It is further extended to cancel the $kT/C$ noise in CDS mode. A prototype ADC in 180nm CMOS occupies only 9.3$\mu$m x 830$\mu$m. It achieves 60.5dB SNR after CDS with 256kHz sampling frequency and 91$\mu$W power consumption.

This chapter is organized as follows: The schematic design of the proposed SAR/SS ADC is first presented. The implementation of the circuit is explained next. The measurement results are shown, followed by the conclusion.

## 4.1 Introduction

In CMOS image sensors, single-slope (SS) ADCs are widely used in column-parallel architectures. It offers good linearity and has a simple architecture [Yoshihara et al. [2006]]. It mainly consists of a single comparator with the small area. However,

conversion speed is a limiting factor in high-bit resolution since more than $2^N$ cycles are required for a N-bit resolution. 1-bit increase in the resolution makes the quantization period double. Therefore, for high resolution, it requires a fast clock speed, leading to the higher power consumption.

To overcome the speed disadvantage, other ADC schemes for column-parallel architectures have been suggested to date. [Snoeij et al. [2007]] divides the input range into $m$. It employs a coarse ramp and $m$ multiple fine ramps in order to perform the two-step quantization. A fine ramp does not need to sweep through all input range, but only $\frac{1}{m}$ span after the coarse ramp determines the input subrange. Although it shortens the conversion period, disadvantage of this work is the necessity of $m$ multiple ramps, which increases the power consumption and nonconformity between fine ramps. Cyclic ADC [M. Furuta and Kawahito [2007]] provides fast operation speed. However, high-performance analog amplifier is required to accomplish high gain and short settling time, which consumes considerable power. $\Delta\Sigma$ ADC is used in [Jo et al. [2016]], but it has the same disadvantage of using the amplifier. Compared with the cyclic ADC, successive approximation register (SAR) ADC [Matsuo et al. [2009]] removes the need for the amplifier, which makes it the best power efficient scheme. It, however, requires accurate capacitor matching especially in the high-bit application. Accordingly, its chip area becomes very large, which is not appropriate for the column-parallel architecture. To solve this issue, two-step approach combining SAR ADC and SS ADC is proposed in [Tang et al. [2013]]. 3-bit SS conversion is first performed and then 8-bit SAR conversion follows. Since 3 MSB bits are determined by SS, the total capacitance for

SAR can be reduced. Therefore, the area becomes smaller than 11-bit SAR ADC. However, high and low reference voltages for SAR must be adjusted according to the input subranges from the SS results. This means that many variable and accurate voltage references must be required. Another disadvantage is that two separate comparators are used for SS and SAR, which may cause the offset.

In this chapter, a two-step quantization ADC of 4-bit SAR + 8-bit SS topology is presented. 4 MSB bits are determined by SAR ADC and the residue is dealt with SS ADC. The proposed architecture incorporates SS ADC to SAR ADC with no extra hardware cost except the ramp generator that is shared globally to all column-parallel ADCs. One continuous comparator is used for both quantization schemes with analog CDS technique. Since only 4 bits are converted by SAR, the area of the capacitor array is smaller while taking advantage of the shorter conversion time of SAR. Even though one cycle of SAR needs longer time than that of SS, it still offers greatly reduced conversion time in comparison with the sole SS ADC. In addition, CDS that is wildly adopted in ADCs for CIS are exploited to reduce the thermal noise of the ADC. As the $kT/C$ noise limits the resolution, the capacitance must be big for high-bit resolution. Therefore, $kT/C$ noise cancellation helps to further relax the requirement of the total capacitor area. It is noted that [Kim et al. [2016]] independently suggested the SAR/SS ADC. In our work, analog CDS is used to implement the dual CDS. This helps to reduce the digital measurement range of the offset in the pixel reset phase [Yoshihara et al. [2006]]. Another is to exploit the CDS to cancel the $kT/C$ noise. With this technique, capacitor size can be smaller than the target resolution, resulting in the smaller area

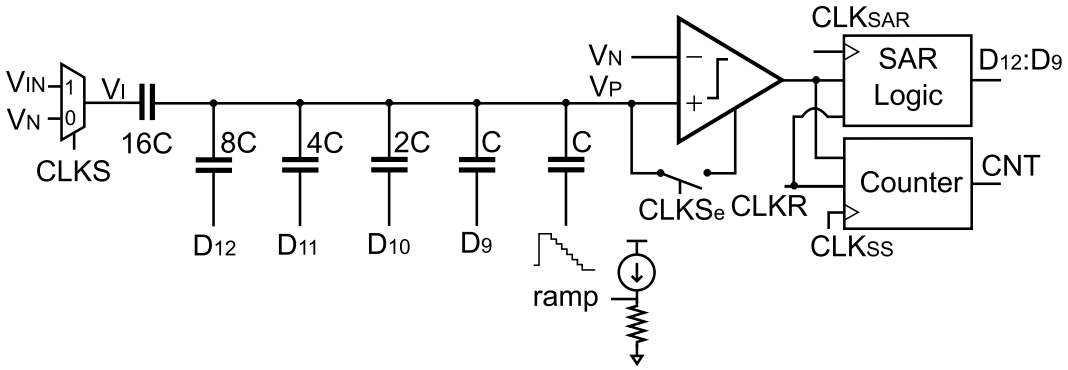


Figure 4.1: Architecture of the proposed SAR/SS ADC.

and less power consumption.

A prototype ADC designed in 180nm occupies 9.7$\mu$m x 830$\mu$m. It achieves 56.3dB SNDR while sampling at 256kHz and consuming only 91$\mu$W. After CDS, the remaining noise is measured to be 0.56LSB, which gives 60.5dB SNDR, 4dB improvement.

## 4.2 Proposed ADC Architecture

Fig. 4.1 shows the proposed two-step SAR/SS ADC architecture employing 4-bit SAR and 8-bit SS quantization. Conventional binary-weighted capacitive DAC array is used for 4-bit MSB SAR conversion. For SS, one unit capacitor ($C$) is connected to a ramp generator block. A comparator is shared. Therefore, adding SS to SAR does not require additional hardware. Separate clocks ($CLK_{SAR}$ and $CLK_{SS}$) are applied to each step. Input capacitor is for the analog CDS and noise cancellation, which will be explained later. A multiplexer (MUX) is located prior to the input capacitor. In the image sensor, there would be image pixels connected to

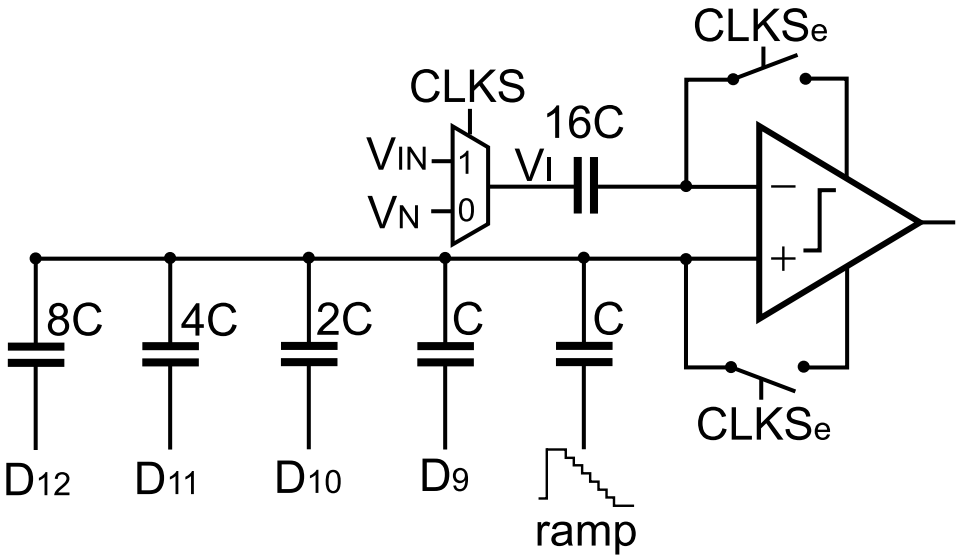


Figure 4.2: Alternative architecture of SAR/SS ADC.

the input capacitor. However, in this implementation, MUX is placed for sampling instead of the image pixel since a photo diode was not offered in the process used. Comparison voltage of the comparator is the same as $V_N$, one of the MUX inputs. It is noted that input is assumed to be above $V_N$.

There can be an alternative architecture (Fig. 4.2). In this architecture, there is no input attenuation. Fig. 4.1 suffers the input attenuation by 2 due to the ratio of the input capacitance to the total DAC capacitance. However, Fig. 4.1 has following advantages. Since the comparison voltage ($V_N$) is fixed, comparator does not need large common mode rejection, which leads to simpler comparator design with the low input swing . Furthermore, single-slope crossing voltage, $V_N$, is also signal independent. And linearity is not degraded by nonlinear capacitors at two comparator inputs. However, owing to the signal attenuation, care must be taken

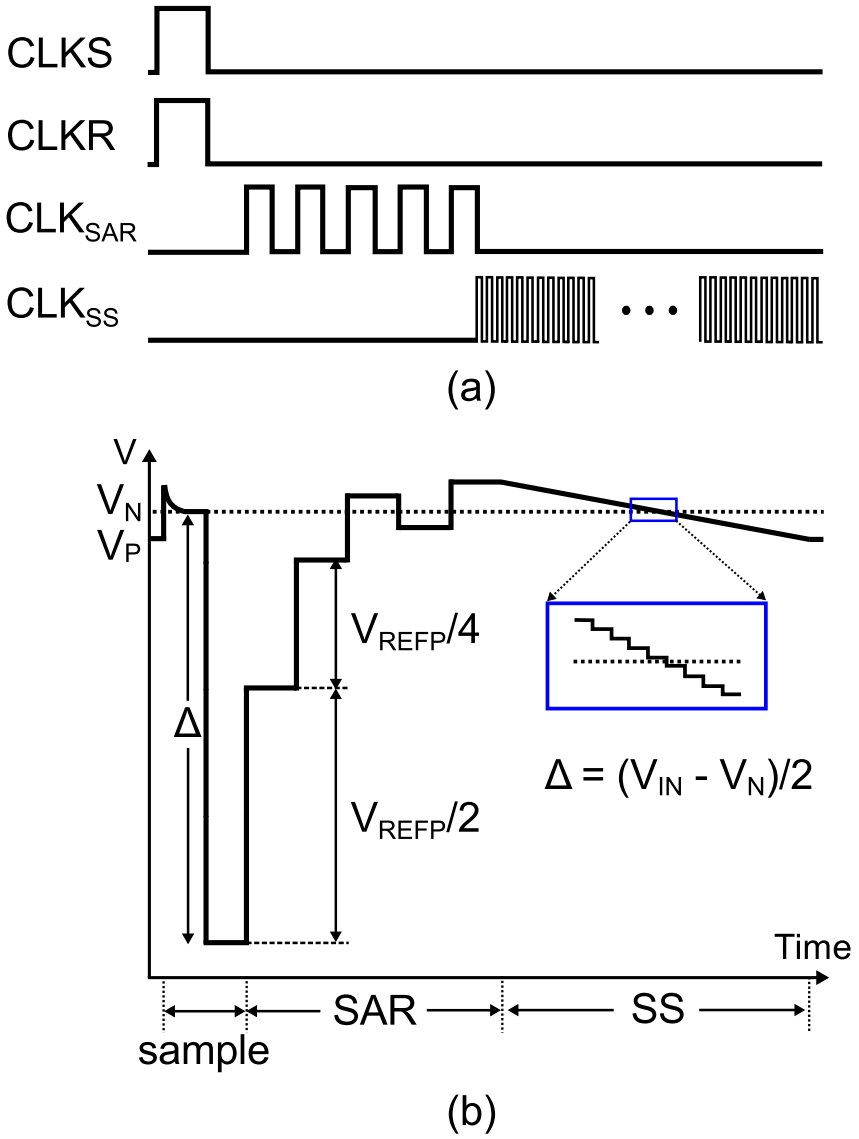


Figure 4.3: (a) Timing diagram, (b) Behavior of $V_P$.

for the comparator design for the low input-referred noise.

Fig 4.3 describes a timing diagram of the ADC and behavior of the $V_P$ node voltage. First, difference of $V_{IN}$ and $V_N$ is sampled on $CLKS$ and ac-coupled to

$V_P$ node through an input capacitor with the attenuation by 2. At the same phase, $CLKR$ resets the SAR logic and the counter. During sampling, early $CLKS$ ($CLKS_e$) turns on the switch to store the comparator offset at the input capacitor for analog CDS. At the same time, this provides the DC bias to the $V_P$ node. Since $V_P$ is in the middle of the capacitors, DC bias must be supplied. Feedback around the first stage of the comparator works in a such way that $V_P$ becomes the same as $V_N$. Offset may exist, but it is canceled by the analog CDS. $CLKS_e$ goes low slightly earlier than $CLKS$ in the bottom-plate sampling way. After sampling, charge stored at $V_P$ is converted by SAR and SS. Conventional DAC switching technique is used. At the SAR phase, ramp signal is fixed to the certain DC, which will be explained. As the input signal, reference voltage is also attenuated by 2. As can be seen in the Fig. 4.3, each DAC reference voltage goes high first sequentially and is chosen high until $V_P$ crosses $V_N$. After 4 cycles, first 4 MSBs are determined. Then next quantization by SS begins. Since ramp only decreases, $V_P$ must be larger than $V_N$. Therefore, the ramp signal goes up to the full ramp voltage in the first place, which requires some time for $V_P$ to settle. Same period of one SAR cycle is allocated for settling. Ramp decreases while a counter block counts until $V_P$ crosses $V_N$. Due to the mismatches between capacitors, $V_P$ may not go over $V_N$ at the start of SS phase. Thus, ramp range should be larger than LSB of SAR.

In CIS, CDS is adopted to cancel any offset of the readout path. It also cancels the reset noise of the image pixel. Owing to the consecutive conversion after reset, the reset noise in two samples is correlated. This means that by subtracting two samples, reset noise as well as offset can be canceled out. This can be extended

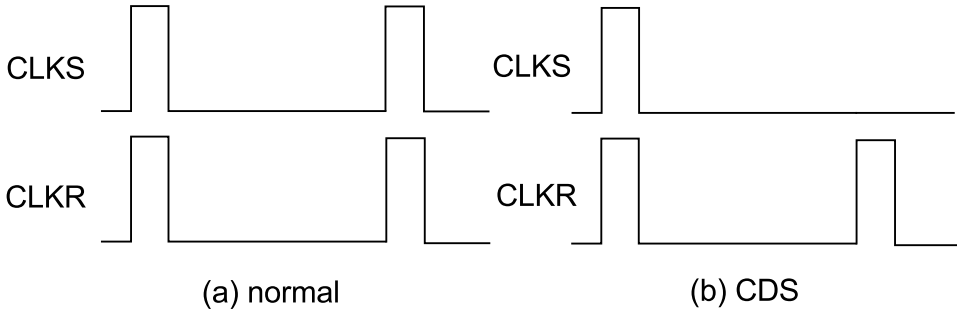


Figure 4.4: CLKS and CLKR in (a) a normal operation, (b) CDS.

to the cancellation of $kT/C$ noise in the proposed architecture. After sampling, $kT/C$ noise is stored at $V_P$ node. Consecutive two conversions after sampling do not change the $kT/C$ noise. This means that $kT/C$ noise sampled is correlated and can be canceled by CDS. Therefore, $kT/C$ noise can be larger than the design specification, which results in the relaxed requirement for the total capacitance, leading to the smaller area. Furthermore, smaller capacitance makes the settling of the reference voltage in SAR faster. However, in the proposed scheme, the input signal also gets canceled by CDS. The final resolution is estimated from the uncanceled noise. The uncanceled noise is measured by converting the sampled input two times and subtracting one from the other.

Timing for normal and CDS operation is shown in Fig. 4.4. In Fig. 4.4(a), sampling is performed every time. In Fig. 4.4(b), input is sampled one time and then converted two times. In this consecutive conversion, $CLKR$ resets the SAR logic and SS logic for ramp, which sets $V_P$ back to the point right after sampling (Fig. 4.3(b)). As mentioned previously, sampling noise is correlated to each conversion. Therefore, remaining uncanceled noise after subtraction is less than the noise in a

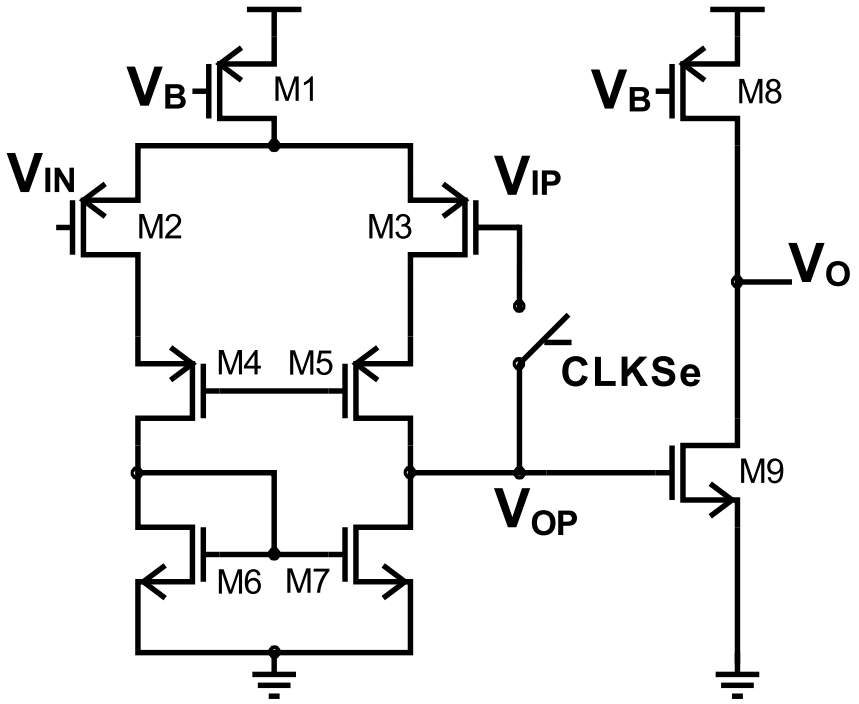


Figure 4.5: Schemtaic of the continuous comparator

normal operation.

## 4.3 Circuit Implementation

Fig. 4.5 shows the continuous comparator design. It includes a differential pre-amplifier followed by a single-ended common-source amplifier. Strong-arm latch is avoided at the cost of the slower speed due to its dynamic behavior which causes power noise crosstalk to the neighboring column-parallel ADCs. PMOS input pair is chosen due to its superior flicker noise characteristic in comparison with the NMOS input pair. The node $V_{IN}$ is connected to the $V_N$ in Fig. 4.1, and the node $V_{IP}$ to the $V_P$. During the sampling period, $CLKS_e$ is high to provide

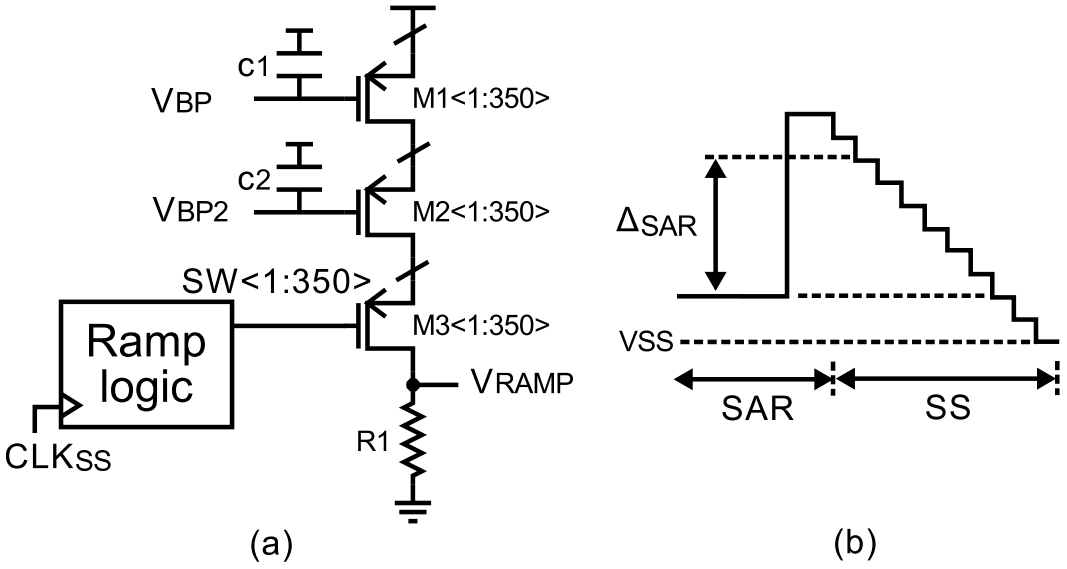


Figure 4.6: (a) Schematic of the ramp generator, (b) VRAMP behavior

the bias to $V_P$ node since the node $V_P$ is ac-coupled to the input and SAR reference voltages and is not connected directly to the DC bias. It also gives the benefit of input offset cancellation by storing the comparator offset across the input capacitor during sampling. M4 and M5 are inserted as abrupt change of $V_P$ during SAR operation causes huge coupling to $V_{OP}$ node, which leads to the conversion error. However, this induces higher gain and lower 3-dB bandwidth. Therefore, settling time becomes longer.

A ramp generator for the single-slope ADC is represented in Fig. 4.6(a). PMOS current sources (M1) and switches (M3) are used in a ramp generator. Switches control the current through the resistor which sets the voltage at the output node ($V_{RAMP}$). M2 is inserted to suppress the coupling from $SW$ signals to $V_{BP}$. This interference can cause the fluctuation of $V_{BP}$, causing the unwanted current

change. Since this output is shared through all column-parallel ADCs, resistance must be low so as to have small RC constant. Currently 500 ohm is chosen. To absorb the power and prevent kickback noise from the high swing input of $SW$ signals, a large capacitor is located between power supply and $V_{BP}$ and $V_{BP2}$. $SW$ signals are generated by DFFs in the ramp logic block.

Redundancy of the ramp is illustrated in Fig. 4.6(b). Mismatch of the capacitors causes an offset that may be bigger than the desired magnitude of LSB of SAR. This must be dealt with. Redundancy can be added to SAR or SS. However, redundancy in SAR usually needs one more capacitor and cycle, which might not be appropriate as it consumes area and waste conversion time. Because area restriction is tough in this application, redundancy in single-slope is a better choice. Even though this needs more current sources in a ramp generator, the ramp is shared to all ADCs so area penalty is small. In this circuit, 94 more current sources are added to 256 current sources in both lower and upper direction. It operates as follows (Fig. 4.6(b)). Ramp voltage is set to the voltage of $47 \times I_{RAMP}$ during sampling/SAR operation and jumps to $350 \times I_{RAMP}$ by turning on all current sources after first 4 SAR cycles. One more cycle is allocated for settling. Then ramp moves downward.

SAR logic is divided into two according to the global and local operation to save the area. On each SAR cycle, a reference voltage is applied to each capacitor, and the final DAC voltage is determined based on the comparison result. The former is the same to all column-parallel ADCs, therefore this part can be a global block. For the counter, ring counter is used since it requires only one clock. This leads to the small power consumption and less clock routing complexity.

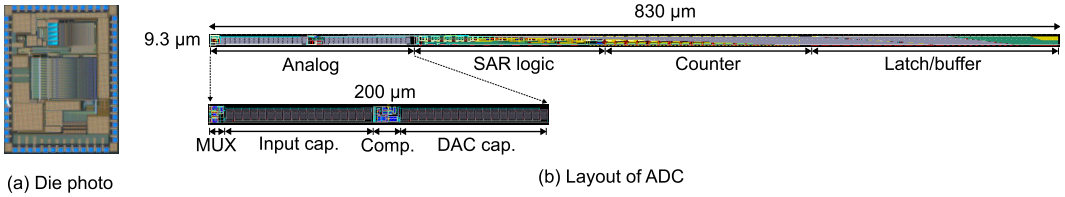


Figure 4.7: (a) Die photo, (b) Layout of the SAR/SS ADC

## 4.4 Measurement

The prototype ADC is fabricated in 180nm CMOS and occupies an area of 9.3$\mu$m x 830$\mu$m as shown in Fig. 4.7. Fig 4.7(a) shows the chip die photo. It consists of 50 ADCs in a column-parallel architecture and a ramp generator. Fig. 4.7(b) illustrates the layout of the single-channel SAR/SS ADC. Analog blocks including a MUX, a comparator and input/DAC capacitors are 200$\mu$m long. The comparator is placed between the input capacitor and DAC capacitors. MOM cap is used and unit cap size is 10fF. Total capacitance is around 320fF. Latches and buffers are needed for output selection among column-parallel ADCs. Analog and digital power supplies are 2.8V and 1.8V, respectively. Input range is 1.25V and is assumed to be over 1.0V ($V_N$). This is reasonable as the reset voltage of the pixel is close to the power supply. In this measurement, SAR and SS clocks are 3.5MHz and 175MHz, respectively, which gives 256kHz conversion speed.

Time domain outputs are plotted in Fig. 4.8. Fig 4.8(a) is the reconstructed SAR output in the voltage domain. Output of the counter in the SS conversion is shown in Fig. 4.8(b). 1 count number corresponds to the 1 step in ramp. Due to the larger-than-expected parasitic capacitance between the comparator and the counter (Fig. 4.7(b)), it takes many clock cycles for the comparator output to stop the

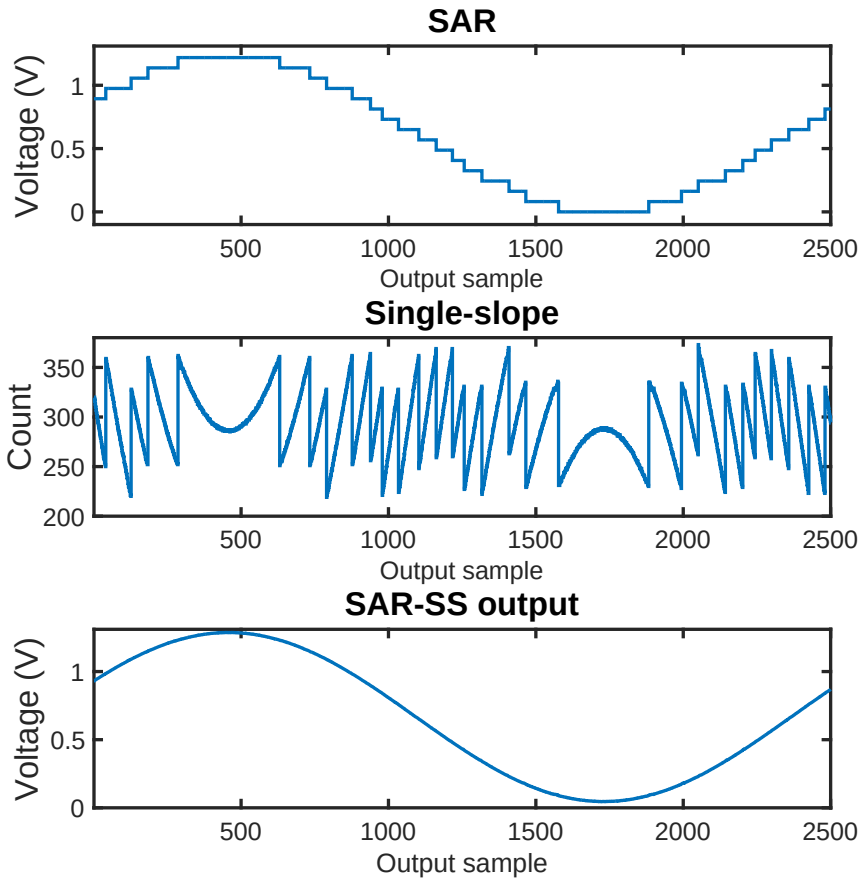


Figure 4.8: Plots of (a) SAR, (b) single-slope, and (c) the reconstructed output

counter. This is reflected in Fig. 4.8(b). As can be seen, count spans between 220 and 360. Since the ideal minimum number is around 50 as explained in the previous section, high number of the minimum count means that transition of the comparator output is slower than estimation due to the large parasitic capacitance. In order to constrain the maximum count of the output within the range of the ramp, resolution of SS was diminished by increasing the ramp step size. The difference is 140, not

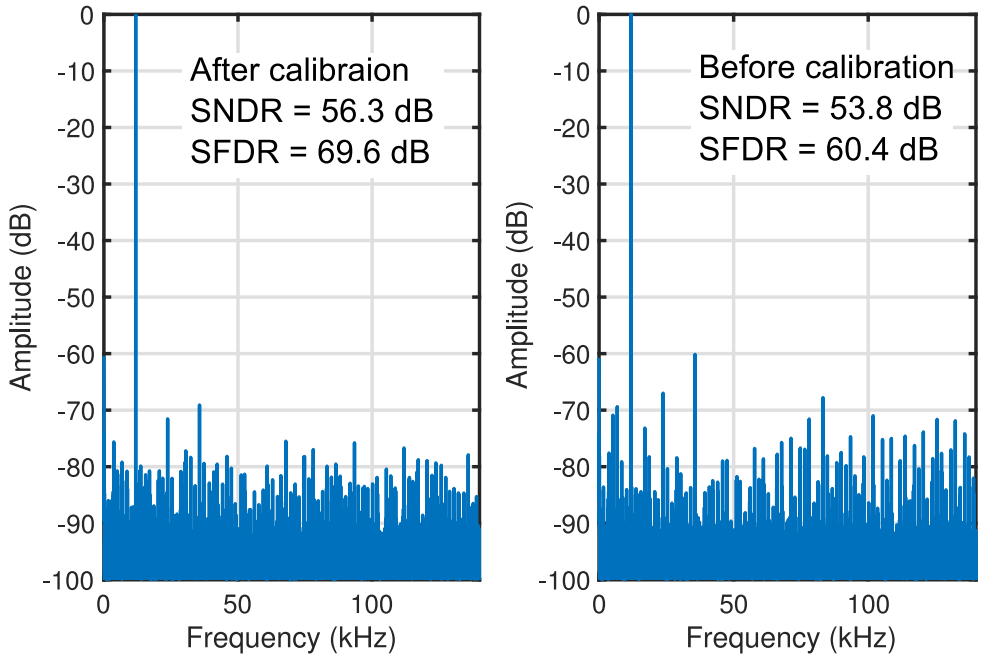


Figure 4.9: Measured ADC spectrum (a) before, and (b) after calibration.

256 of 8-bit, which results in 1-bit loss. Therefore, gain between two quantization schemes must be adjusted according to this discrepancy. Reconstructed output from SAR and SS results are illustrated in Fig. 4.8(c).

Fig. 4.9 shows the measured FFT spectrum with 256kHz sampling rate and 11kHz input. Capacitor mismatch and gain mismatch between two conversion are calibrated in the foreground fashion. FFT results after and before calibration are compared. As shown in the plots, harmonics decrease after calibration. SFDR improves by 9dB. Note that the circuit is designed to have SNDR lower than the target resolution to save the area of capacitors. By exploiting the correlated $kT/C$ noise cancellation by CDS, SNDR improvement can be anticipated. This is confirmed

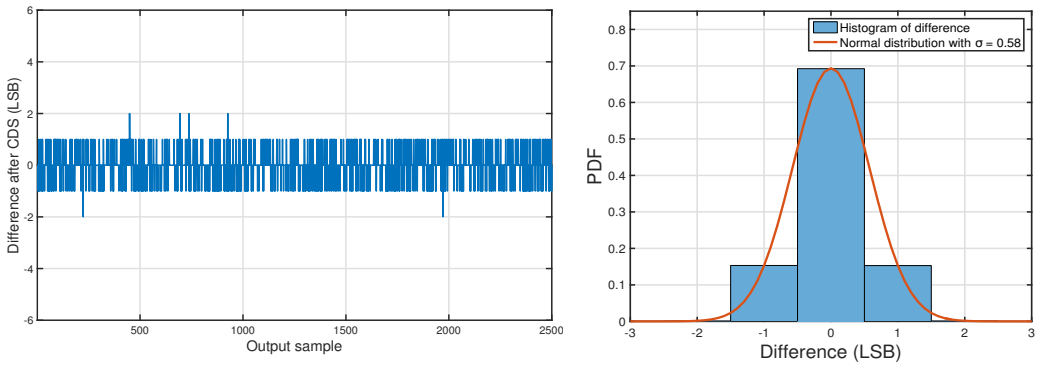


Figure 4.10: (a) Output after CDS, (b) Histogram of output

by Fig. 4.10. Outputs are measured with DC input in order to convert the same input multiple times. Fig. 4.10(a) shows the difference after CDS in LSB scale with the DC input. Ideal plot is 0 along all output samples. From Fig. 4.10(b), measured standard deviation is 0.56LSB, which is 440$\mu V_{rms}$. This corresponds to SNDR of 60.4dB with 1.3V input range. 3 4dB improvement is achieved. Effective number of bits (ENOB) is estimated to be about 9.74-bit. Here, digital CDS is not implemented. It is performed off-chip.

Measured DNL and INL are -0.96/1.44 LSB and -2.29/1.51 LSB respectively in 10-bit scale. (Fig. 4.11). The total power consumption is 91$\mu$W, whose breakdown is : 6$\mu$W used by analog blocks, 85 $\mu$W by digital blocks. Table 4.1 compares this work with other works.

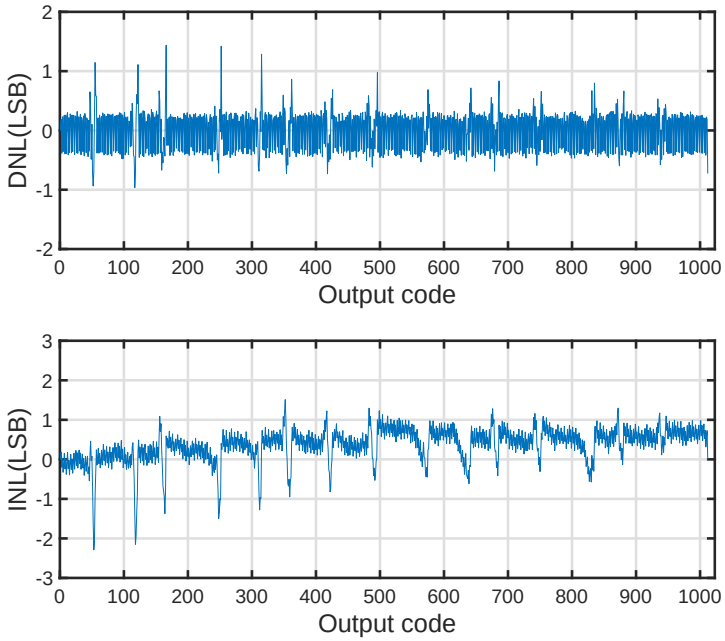


Figure 4.11: DNL and INL plots

Table 4.1: Comparison with other column-parallel ADCs for CIS

| | **This work** | Snoeij et al. [2007] | Matsuo et al. [2009] | Tang et al. [2013] | Kim et al. [2016] |
|---|---|---|---|---|---|
| Process (nm) | **180** | 250 | 180 | 130 | 90 |
| Architecture | **SAR/SS** | Multi SS | SAR | SS/SAR | SAR/SS |
| Area ($\mu m^2$) | **9.7x800** | - | 8.4x1320 | 7x1100 | 2.2x998 |
| Conversion time ($\mu$s) | **3.87** | 16 | 1.7 | 12 | 2.7 |
| ENOB/resolution (bit) | **9.7/12** | -/10 | -/14 | 6.4/11 | -/12 |
| Power ($\mu$W) | **91** | 68 | 41 | 4 | 30 |

## 4.5 Conclusion

This chapter presented a two-step SAR/SS ADC for column-parallel ADCs for CIS. SS ADC is added to SAR ADC with the minimal modification. By adopting the SS, total capacitance of SAR can be reduced while taking advantage of the fast conversion speed of SAR. Analog CDS is applied to cancel the offset of the comparator. Furthermore, it is employed to improve the resolution by using the correlated nature of the $kT/C$ noise after sampling.

# Chapter 5

# Conclusions and Future Directions

## 5.1 Conclusions

Advanced design techniques to address the current limitation are developed for three types of ADCs : (1) high-speed SAR ADC, (2) continuous-time $\Delta\Sigma$ ADC, (3) single-slope ADC for CMOS image sensors. Each prototype ADC was fabricated and measured to validate the proposed techniques.

Chapter 2 presented a sparkle code reduction technique along with the resolution enhancement. Comparator decision time detector is inserted to monitor the metastability event. Dither-based background calibration is proposed to adjust the detection window to be half LSB, which leads to the 1-bit resolution enhancement. This technique can reduce the total comparison cycles by 1. This cycle reduction saves the power accordingly. Furthermore, comparator requirement to have a low BER is relaxed by the proposed technique.

Chapter 3 presented a continuous-time $\Delta\Sigma$ ADC with VCO-based integrators. It can replace the power-hungry op amp within the $\Delta\Sigma$ loop by converting the data in the phase domain. On top of the inherent DEM property, which comes from the dual-VCO-based architecture, a novel DAC calibration technique is applied to relax the strict mismatch requirement on DACs in the feedback path. This makes

the small area of DACs possible to enable a compact layout. Distributed modular design, which is digital-friendly, is done utilizing the proposed technique. This low-power benefit of VCO increases further as the technology scales. Chapter 3 also extends the work to the second-order single-loop purely-VCO-based $\Delta\Sigma$ ADC in the behavior simulation. PWM property of the VCO-based integrator is analyzed and used.

Chapter 4 showed the two-step ADCs by incorporating SAR into SS ADC. The proposed two-step ADC shortens the conversion speed. In the proposed architecture, $kT/C$ noise cancellation through the analog correlated-double sampling relieves the limitation of DAC area of SAR ADC.

## 5.2 Future Directions

The proposed dither-based sparkle code reduction technique can be applied to the high-speed SAR ADCs. To this end, comparator and dynamic SAR logic gates must be designed well in deeply scaled CMOS process since the current speed limitation comes from the both. In addition, in order to use the complementary behavior of the comparator decision time and DAC settling time fully, synchronous clocking can be applied instead of the asynchronous scheme. Although power consumption of the clock network becomes more, it can operate faster due to the reduced loading of the NOR gate. Furthermore, conversion can be stopped after the metastability detection to further decrease the power. However, in a high speed SAR ADC, it is not easy to stop the conversion right after metastability occurrence owing to the time needed to check the detection results and to stop the clocking

loop.

For the $\Delta\Sigma$ ADC, with the proposed distributed modular architecture, continuous-time $\Delta\Sigma$ ADC can be easily reconfigured based on the resolution requirement. Also, layout can be automated if the slice is set as a basic building block. Due to the proposed DAC calibration which solves the DAC nonlinearity, the size of the slice having DAC inside can be smaller in the advanced CMOS process.

Two-step SAR/SS ADC can be more optimized to have the best performance considering the trade-off between SAR and SS ADCs. $kT/C$ noise cancellation is more actively exploited to further decrease the DAC capacitance. Since input and DAC capacitors take huge area and put the stringent area limitation on the layout, reduced DAC capacitance as well as input capacitance makes the SAR/SS ADC smaller. However, since the capacitors should have higher-than the 12b accuracy, unit capacitor size and layout should be considered well to reduce the capacitor mismatch. Clocked comparator is also used to make it faster. Continuous comparator that is currently employed takes a longer time to resolve the output while the counter keeps counting. Thus, by using the clocked comparator, output resolving time can be shorter. However, in this case, power fluctuation may be worse. Therefore, shielding between the neighboring column-parallel ADCs should be done carefully.

# Appendix

# Appendix 1

# List of Publications

1. **Yeonam Yoon**, and Nan Sun, "A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration," accepted to IEEE Custom Integrated Circuits Conference (CICC), 2017.

2. Long Chen, Xiyuan Tang, Arindam Sanyal, **Yeonam Yoon**, Jie Cong, and Nan Sun, "A 0.7V 0.6W 100kS/s Low-Power SAR ADC with Statistical Estimation Based Noise Reduction," accepted to IEEE Journal of Solid-State Circuits 2017.

3. Miguel Gandara, Wenjuan Guo, Xiyuan Tang, Long Chen, **Yeonam Yoon**, and Nan Sun, "A Pipelined SAR ADC Reusing the Comparator as Residue Amplifier," accepted to IEEE Custom Integrated Circuits Conference (CICC), 2017.

4. Kyoungtae Lee, **Yeonam Yoon**, and Nan Sun, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," IEEE Journal of Emerging and Selected Topics in Circuits and Systems, vol. 5, no. 4, pp. 561-573, Dec. 2015.

5. **Yeonam Yoon**, Koungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen, and Nan Sun, "A 0.04-$mm^2$ Modular $\Delta\Sigma$ ADC with VCO-based Integrator and 0.9-mW 71-dB SNDR Distributed Digital DAC Calibration," Custom Integrated Circuit Conference (CICC), pp. 1-4, Sep. 2015.

6. Long Chen, Xiyuan Tang, Arindam Sanyal, **Yeonam Yoon**, Jie Cong, and Nan Sun, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction," IEEE Custom Integrated Circuit Conference (CICC), pp. 1-4, Sep. 2015.

7. **Yeonam Yoon**, Kyoungtae Lee, and Nan Sun, "A purely-VCO-based single-loop high-order continuous-time delta sigma ADC," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 926-929, 2014.

8. Kyoungtae Lee, **Yeonam Yoon**, and Nan Sun, "A 1.8mW 2MHz-BW 66.5dB-SNDR delta-sigma ADC using VCO-based integrators with intrinsic CLA," IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, 2013

9. Kyoungtae Lee, **Yeonam Yoon**, and Nan Sun, "A 10MHz-BW, 5.6mW, 70dB SNDR $\Delta\Sigma$ ADC using VCO-based integrators with intrinsic DEM," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2006 2009, 2013.

## Future publications

1. Yeonam Yoon, and Nan Sun, "A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration," to be submitted to IEEE Journal of Solid-State Circuits (JSSC).

2. Yeonam Yoon, and Nan Sun, "SAR/Single-Slope Two-Step Quantization for CMOS Image Sensor Exploiting KT/C Noise Cancellation by Correlated Double Sampling," to be submitted to IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II).

# Bibliography


L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici. A 90GS/s 8b 667mW 64x interleaved SAR ADC in 32nm digital SOI CMOS. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 378–379, 2014.

C. H. Chan, Y. Zhu, I. M. Ho, W. H. Zhang, S. P. U, and R. P. Martins. A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration. In *2017 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 282–283, 2017a.

Y. Z. Lin, C. H. Tsai, S. C. Tsou, and C. H. Lu. A 8.2-mW 10-b 1.6-GS/s 4x TI SAR ADC with fast reference charge neutralization and background timing-skew calibration in 16-nm CMOS. pages 1–2, 2016.

S. Guhados, P. J. Hurst, and S. H. Lewis. A pipelined ADC with metastability error rate $< 10^{-15}$ errors/sample. *IEEE Journal of Solid-State Circuits*, 47(9): 2119–2128, 2012.

O. E. Agazzi. A 90 nm CMOS DSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multi-mode optical fibers at 10 Gb/s. *IEEE Journal of Solid-State Circuits*, 43(12):2939–2957, 2008.

S. Hashemi and B. Razavi. Analysis of Metastability in Pipelined ADCs. *IEEE Journal of Solid-State Circuits*, 49(5):1198–1209, 2014.

A. Waters, J. Muhlestein, and U. Moon. Analysis of metastability errors in conventional, LSB-fisrt, and asynchronous SAR ADCs. *IEEE Transactions on Circuits and Systems-I: Regular Papers*, 47(4):1022–1030, 2012.

C. H. Chan, Y. Zhu, S. W. Sin, B. Murmann, S. P. U, and R. P. Martins. Metastablility in SAR ADCs. *IEEE Transactions on Circuits and Systems-II: Express Briefs*, 64(2):111–115, 2017b.

S. W. Chen and R. Brodersen. A 6b 600MS/s 5.3mW asynchronous ADC in 0.13$\mu$m CMOS. In *2006 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 2350–2359, 2006.

C. Chan, Y. Zhu, S. Sin, S. U, and R. P. Martins. A 5.5mW 6b 5GS/s 4x-interleaved 3b/cycle SAR ADC in 65 nm CMOS. In *2015 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 466–468, 2015.

J. P. Keane, N. J. Guilar, D. Stepanovic, B. Wuppermann, C. Wu, C. W. Tsang, R. Neff, and K. Nishimura. An 8GS/s time-interleaved SAR ADC with unresolved decision detection achieving -58dBFS noise and 4GHz bandwidth in 28nm CMOS. In *2017 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 284–286, 2017.

Y. Duan and E. Alon. A 6b 46GS/s ADC with >23GHz BW and sparkle-code error correction. In *2015 Symposium on VLSI Circuits (VLSI Circuits)*, pages C162–C163, 2015.

A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro. A 0.5V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS. *IEEE Journal of Solid-State Circuits*, 47(4):1022–1030, 2012.

R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu. A 14b 80 MS/s SAR ADC With 73.6 dB SNDR in 65 nm CMOS. *IEEE Journal of Solid-State Circuits*, 48(12):3059–3066, 2013.

C. Liu, S. Chang, G. Huang, Y. Lin, and C. Huang. A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18$\mu$m CMOS. In *2010 Symposium on VLSI Circuits (VLSI Circuits)*, pages 241–242, 2010.

D. Shinkel, E. Menshink, E. Klumperink, E. van Tuijl, and B. Nauta. A double-tail latch-type voltage sense amplifier with 18ps setup+hold time. In *2007 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 314–315, 2007.

K. Choo, J. Bell, and M. Flynn. Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based DAC. In *2016 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 460–462, 2007.

T. Jiang, W. Liu, F. Y. Zhong, C. Zhong, K. Hu, and P. Y. Chiang. A single-channel, 1.25-GS/s, 6-bit, 6.08-mW asynchronous successive-approximation ADC with improved feedback delay in 40-nm CMOS. *IEEE Journal of Solid-State Circuits*, 47(10):2444–2453, 2012.

G. Taylor and I. Galton. A reconfigurable mostly-digital $\Sigma\Delta$ ADC with a worst-case FOM of 160dB. *IEEE Journal of Solid-State Circuits*, 48(4):983–995, 2013.

K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P.K. Hanumolu. 16-mW 78-dB SNDR 10-MHz BW CT ADC using residue-cancelling VCO-based quantizer. *IEEE Journal of Solid-State Circuits*, 47(12):2916–2927, 2012.

M. Z. Straayer and M. H. Perrot. A 12-bit 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-Bit 950-MS/s VCO-based quantizer. *IEEE Journal of Solid-State Circuits*, 43(4):805–814, 2008.

K. Lee, Y. Yoon, and N. Sun. A 1.8mW, 2MHz-BW 66.5dB-SNDR delta-sigma ADC using VCO-based integrators with intrinsic CLA. In *2013 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–4, 2013a.

M. Park and M. H. Perrot. A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Sigma\Delta$ ADC with VCO-based integrator and quantizer implemented in 0.13 $\mu$m CMOS. *IEEE Journal of Solid-State Circuits*, 44(12):3344–3358, 2009.

S. Rao, K. Reddy, B. Young, and P.K. Hanumolu. A deterministic digital background calibration technique for VCO-based ADCs. *IEEE Journal of Solid-State Circuits*, 49(4):950–960, 2014.

B. Young, K. Reddy, S. Rao, A. Elshazly, T. Anand, and P. K. Hanumolu. A 75dB DR 50MHz BW 3rd order CT-$\Delta\Sigma$ modulator using VCO-based integrators. In *2014 Symposium on LSI Circuits (VLSI Circuits)*, pages 1–2, 2014.

J. G. Kauffman, P. Witte, M. Lehmann, J. Becker, Y. Manoli, and M. Ortmanns. A 72dB DR, CT $\Sigma\Delta$ modulator using digitally estimated auxiliary DAC linearization achieving 88fJ/conv-step in a 25 MHz BW. *IEEE Journal of Solid-State Circuits*, 49(2):392–404, 2014.

S. Yan and E. Sanches-Sinencio. A continuous-time $\Sigma\Delta$ modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth. *IEEE Journal of Solid-State Circuits*, 39(1):75–86, 2004.

G. Taylor and I. Galton. A mostly-digital variable-rate continuous-time delta-sigma modulator ADC. *IEEE Journal of Solid-State Circuits*, 45(12):2634–2646, 2010.

K. Lee, Y. Yoon, and N. Sun. A 10MHz-BW, 5.6mW, 70dB SNDR $\Sigma\Delta$ ADC using VCO-based integrators with intrinsic DEM. In *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2006–2009, 2013b.

L. Hernandez. VCO based multi-stage noise shaping ADC. *Electronics Letters*, 48 (4):206–208, 2012.

W. Yu, J. Kim, K. Kim, and S. Cho. A time-domain high-order MASH $\Sigma\Delta$ ADC using voltage-controlled gated-ring oscillator. *IEEE Transactions on Circuits and Systems-I: Regular Papers*, 60(4):856–866, 2013.

S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P.K. Hanumolu. A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation. In *2011 Symposium on VLSI Circuits (VLSI Circuits)*, pages 270–271, 2011.

S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto. A 1/1.18-inch 6.4 MPixel 60 frames/s CMOS image sensor with seamless mode change. *IEEE Journal of Solid-State Circuits*, 41(12):2998–3006, 2006.

M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing. Multiple-ramp column-parallel ADC architecture for CMOS image sensors. *IEEE Journal of Solid-State Circuits*, 42(12):2968–2977, 2007.

T. Inoue M. Furuta, Y. Nishikawa and S. Kawahito. A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters. *IEEE Journal of Solid-State Circuits*, 42(4):766–774, 2007.

Y. Jo, S. Hong, and O. Kwon. A low-noise and area-efficient PWM-$\Delta\Sigma$ ADC using a single-slope quantizer for CMOS image sensors. *IEEE Transactions on Electron Devices*, 63(1):168–173, 2016.

S. Matsuo, T. J. Bales, M. Shoda, S. Osawa, K. Kawamura, A. Andersson, M. Haque, H. Honda, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi. 8.9-megapixel video image sensor with 14-b column-parallel SA-ADC. *IEEE Transactions on Electron Devices*, 56(11):2380–2389, 2009.

F. Tang, D. G. Chen, B. Wang, and A. Bermak. Low-power CMOS image sensor based on column-parallel single-slope/SAR quantization scheme. *IEEE Transactions on Electron Devices*, 60(8):2561–2566, 2013.

M. Kim, S. Hong, and O. Kwon. An area-efficient and low-power 12-b SAR/single-slope ADC without calibration method for CMOS image sensors. *IEEE Transactions on Electron Devices*, 63(9):3599–3604, 2016.

# Vita

Yeonam Yoon received his B.S. and M.S. degrees from Seoul National University in 2004 and 2008, respectively. His master research topic was on the small-signal modeling of RF CMOS. He worked as a circuit verification/test engineer for Samsung Electronics for 3.5 years from 2008. He joined the ECE department in University of Texas at Austin as a PhD student in fall 2011. He interned in Freescale Semiconductor, Tempe, AZ for 6 months in 2014.

email address: irunjurun@utexas.edu

This dissertation was typeset with LaTeX[†] by the author.

[†]LaTeX is a document preparation system developed by Leslie Lamport as a special version of Donald Knuth's TeX Program.